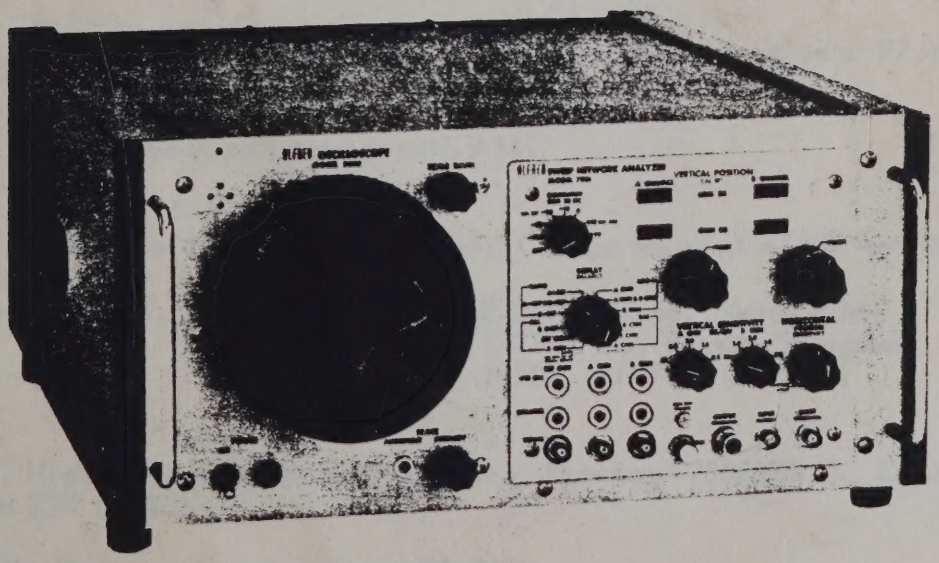
INSTRUCTION MANUAL

sweep network analyzer system

MODEL 8000/7051

Serial _____ _____
8000 7051



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MANUAL CHANGES

FOR

8000/7051
NETWORK ANALYZER

Make corrections to errata listed below and make applicable changes(s) listed in the table below according to instrument serial number.

SERIAL NO.	MAKE CHANGES

SERIAL NO.	MAKE CHANGES

CHANGE 1: Schematic 900824 and Parts List;
Change stock no. for A1Q9, A2Q9, and A3Q9 from 81-268 to 81-113.

Schematic, Sweep Network Analyzer Drawing 900823-3, Rev. G.; Delete jumper wire between pin H and L of A4 (connector J4). This changes the drawing from Rev. G to Rev. J.

CHANGE 2:

A. Schematic, Deflection Circuit, Drawing #900806C-1: Change value of R7 from 2.87K to 2.05K.* (Factory Select)

Add Note 3: Prefix each part number with A14.

B. Parts List, A14 PC Board Assembly, Page 6-7: Change value of A14R7 from 1K to:

Alfred Part No. 56-2.05K — 2.05K, Fixed, Metal Film, 1/2W, 1%, Factory Selected, 19701, MF-7C-TO-2.05K

C. Schematic, High Voltage Regulator & Blanking, Drawing #900807C-1: Change value of R19 from 33K to 220K.

Add Note 3: Prefix each part number with A11.

D. Parts List, A11 PC Board Assembly, Page 6-6: Change value of R19 from 33K to

Alfred Part No. 51-220K — 220K, Fixed, C.F., 1/2W, 5% — 73445 E-009-AB/B-220K

ECO #14832 (A & B)
ECO #14880 (C & D)

April 4, 1973

ERRATA SHEET

Model 8000/7051

Date	ECO#	Effective Serial's	Revision
		All	In Schematic 900824C, the value of resistor R36 should be 619 K, 1%.
	13116	301 & up	On Schematic 900805C-1, add capacitor C11 (0.05 µf) in parallel with R20.
		481 & up	On the A5 parts list, change Alfred Part Numbers as follows: R2 becomes 71-96 R9 becomes 71-91 (applies to R20 also) R11 becomes 71-105 (applies to R17 also)
1-15-68			On page 6-2 of the parts list, change the Alfred Part No. of S4 and S5 to 102-146.
		All	On Schematic 900827C, Terminal Y should be labeled + 126V
4-18-68			On page 6-2 of the parts list, make the following corrections: CR1 thru CR4 should read CR1 thru CR5. On page 6-6 of the parts list, change the wattage ratings of A15R7 and A15R13 to 1/4 watt (1/4 w).
4-25-68		All	In Section 7 on Schematic 900804D draw a connecting line between A13 J2-E and the junction between F2 and R2 (58 Ω).
5-15-68	13566	631 & up	On Pg. 6-6 (A12 Parts List) make the following corrections: A12CR1 81-135 Diode EH400 A12CR5 Same as A12CR1 On Schematic 900804D, Section 7, replace CR1 (dual diode) with 2 seperate diodes, CR1 and CR5. CR1 and CR5 are Diodes EH400. Delete box around these diodes.
5-24-68		All	In the List of Assemblies, Section 6 (p. 6-1) change Alfred Part No. 901226 (A5) to 901299.

MANUAL CHANGES

FOR

MODEL 8000/7051

Make corrections to errata listed below and make applicable changes(s) listed in the table below according to instrument serial number.

SERIAL NO.	MAKE CHANGES

SERIAL NO.	MAKE CHANGES

CHANGE 2:

A. Schematic Deflection Circuit, Dwg #900806C-1:
Change value of R7 from 2.87K to 2.05K*Factory select
ADD: Note 3, Prefix each Part No. with A14.

B. Parts List A14 PC Board Assembly page 6-7
Change value of A14R7 from 1K to:
A Part No.= 56-2.05K 2.05K Fixed Metal Film
1/2W, 1% Factory selected
19701 MF-7C-2.05

ECO#14832

C. Schematic HV Reg & Blanking Dwg No. 900807C-1
Change value of R19 from 33K to 220K
ADD: Note 3, Prefix each Part No. with A11.

D. Parts List A11 PC Boeard Assembly page 6-6
Change value of R19 from 33K to APart No.= 51-220K,
220K, Fixed, C.F. 1/2W, 5% 73445 E-009-AB/B-220K

ECO # 14880

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SECTION 1

GENERAL INFORMATION

1.1 THE ALFRED 8000/7051 SWEEP NETWORK ANALYZER SYSTEM.

The ALFRED Sweep Network Analyzer System consists of the Model 8000 Oscilloscope and the Model 7051 Sweep Network Analyzer Plug-in. This system introduces a new concept in microwave instrumentation: a truly general-purpose instrument that can measure insertion gain or loss, return loss (VSWR) or gain, and absolute or relative levels of CW power over a 60 db dynamic range. The instrument can be used for swept or single-frequency measurements, and also as a dual-channel logarithmic oscilloscope. Functionally, the instrument contains two independent ratiometers with a common reference channel, and a built-in precision rf calibration source. It accepts and processes input signals from up to three standard crystal detectors at separate points in an external rf test circuit, representing two signal levels to be measured (Channels A and B) and a reference signal (Channel REF) for ratio measurements. For absolute level measurements, the Channel A and B detectors are calibrated directly with the built-in rf source. (Special internal circuitry provides accurate compensation for each crystal's departure from square law performance at high levels, to allow direct db measurement over a 60 db range.)

In a typical test application, detectors are inserted in the rf test circuit to provide an indication of incident, reflected, and transmitted signal levels of the device under test. The ratio of reflected to incident power provides a direct indication of return loss (VSWR) or gain (ratio of Channel A to REF Channel). Simultaneously, the ratio of transmitted to incident power provides a direct indication of insertion loss or gain (ratio of Channel B to REF Channel). Direct-reading ratiometer techniques eliminate the time-consuming and error-causing calibration associated with other instruments. When calibrated dbm readout is required, the built-in rf calibration source provides a 60-db range to calibrate the detector at a level equal to that being measured.

The 8000/7051 can be used to make a greater variety of measurements, over a wider dynamic range and a wider frequency spectrum, than any other instrument now available. In addition, measurement speed and simplicity are substantially improved. The use of built-in analog offset controls for each channel eliminates the need for external precision attenuators, and provides greater flexibility by permitting any level of operation to be offset for CRT examination, without attenuating the signal variations displayed. Providing both ratiometric measurements and self-calibrating absolute level measurements, with direct db and dbm readout over a 60-db dynamic range, the 8000/7051 can be used in most microwave measurement applications now requiring one or more of the following instruments: (1) VSWR meter; (2) power meter; (3) logarithmic oscilloscope; (4) lin-log converter; (5) precision attenuator; (6) rf calibration source; and (7) frequency domain reflectometer.

Since the 8000/7051 processes the detected signal from a crystal detector in each measurement channel, the external rf test circuit requires only directional couplers and crystal detectors (or samplers or probes). The instrument is thus not frequency-restricted, except by the availability of suitable crystal detectors and sampling components.

Internal electronic offset permits simple, accurate measurement of input signal characteristics and variations, and provides direct digital readout. An independent front panel Offset control, operating a digital counter which indicates calibrated trace offset to 0.1 db, is provided for each channel.

Signal parameters can be measured with good resolution by comparing any point on the waveform with the calibrated internal offset. A front panel control which disengages the Offset control potentiometer from the digital indicator permits the indicator to be calibrated under zero-set conditions to enable direct readout of the measured parameter.

A major convenience of this internal offset control is that any signal level may be viewed on the CRT regardless of display sensitivity. Thus, any portion of a signal having a large (up to 60 db) dynamic range may be viewed at the maximum display sensitivity of 0.5 db/cm, with proper offset.

The internal offset feature simplifies the external rf test circuit by eliminating the requirement for external precision variable attenuators which add expense and needless frequency restriction in other measurement systems. The offset controls permit any desired level to be offset for on-scale examination without attenuating the signal.

The CRT presentation sensitivity is adjustable over a 20:1 range in db, from 0.5 db/cm to 10 db/cm. A low sensitivity setting permits "quick look" display of wide amplitude variations, and a high sensitivity setting can be used for precision measurement or detailed examination.

1.2 MODEL 8000/7051 PERFORMANCE SPECIFICATIONS.

Specifications of the Model 8000/7051 Sweep Network Analyzer System are given in Table 1-1.

1.3 SCOPE OF THIS MANUAL.

This Instruction Manual covers detailed descriptive data, operating instructions, circuit theory, and servicing information for the Model 8000 Oscilloscope and the Model 7051 Sweep Network Analyzer Plug-in.

1.4 APPLICATIONS OF THE 8000/7051 SYSTEM.

The capability of measuring both ratios and absolute levels over a 60-db range with direct-reading simplicity is a challenge to the ingenious test engineer's imagination. Direct-reading presentation of a simultaneous reflection and transmission performance measurement on nearly any microwave or rf component can be quickly obtained. Similar measurements, or measurements with higher sensitivity, as required for detailed examination, can be made at virtually any point in a microwave or rf system. Thus, the port-to-port performance of individual components or stages, or the overall performance of an entire system can be tested. Even cables can be tested for loss and VSWR, and antennas can be tested for VSWR and pattern. The instrument can be used for routine power level measurements, attenuator calibration, and quick measurement of coupling factor and directivity of couplers and samplers. Detailed applications information is given in Section 3.

Table 1-1. Tentative Specifications of the Model 8000/7051 Sweep Network Analyzer System.

OPERATING FREQUENCY RANGE:	< 100 KHz to > 40 GHz, limited only by availability of suitable crystal detectors and samplers.
MEASUREMENT FUNCTION:	Indicates the ratio of each of two signals to a third (reference) signal directly in db; presents the log of each of two signals linearly; or measures absolute level sensed by crystal detectors on two independent channels.
DYNAMIC RANGE:	Noise level to crystal detector reverse breakdown level (approximately -40 to +20 dbm).
Minimum signal requirement:	A signal of -40 dbm is required at the crystal detector in order for the display to indicate less than 3 db peak-to-peak noise excursion. At signal levels of -30 dbm and higher, noise effects are negligible.
Maximum signal capability:	The voltage breakdown of the crystal detector normally limits the maximum signal that can be applied. Crystal detectors are available from ALFRED to handle signal levels up to +20 dbm.
Square-law compensation:	Special internal circuitry compensates for the crystal law to calibrate the detected output and enable use above the normal square law region, through the linear region to the breakdown level, thereby permitting direct db readout over a 60-db range. A separate calibration adjustment is provided for each detector channel, to permit simple, accurate individual curve-fitting of the compensation characteristic. Compensation accuracy is sufficient to permit over-all system accuracy as specified below.
ACCURACY:	DB measurements: ±0.4 db or ±2% of direct db readout, whichever is greater, when offset method is used. Absolute level measurements: ± DB measurement error from calibration level ± calibrator accuracy at level used. Above specifications apply when using ALFRED Model 1403 Crystal Detector Set. See note at the start of Para. 3.5 (page 3-3), for detector frequency limitations.
INTERNAL RF CALIBRATOR:	Generates 30-MHz signal for detector calibration in 10-db steps from -40 to +20 dbm. Accuracy: ±0.3 db at +20 dbm; ± 0.6 db at all other levels.
READOUT PROVISIONS:	
CRT:	Dual-trace CRT presentation with 0.5 db/cm to 10 db/cm sensitivity, independently adjustable on each channel. CRT face is equipped with a standard 10-cm scribed graticule.
Digital counters:	Direct-reading counter dials on the Offset control for each channel permit direct digital readout in 0.1-db increments, identified as gain or loss.
X-Y recorder drive:	Auxiliary X-Y recorder drive output, linear in db, for permanent recording of single-channel CRT presentations. Deflection sensitivity: 0.2 v/cm (nominal). Output impedance: 10 K. The CRT bezel is designed to accept a standard oscilloscope cameras for permanent photographic recording of single- or dual-channel displays.
INTERNAL LEVEL OFFSET:	60 db of gain or loss, provided independently on each channel by electronic analog techniques; continuously variable with direct-reading counter calibrated in 0.1-db increments.
HORIZONTAL DISPLAY:	The horizontal channel accepts positive sweep inputs ranging from 10 to 50 volts. Front panel controls are provided to position the trace and adjust the horizontal display sensitivity. Minimum sweep time is .01 second. An internal line-frequency sweep is provided to spread the oscilloscope trace during calibration and when making single-frequency or point-by-point measurements.
MARKER INPUT:	Video markers may be applied through the MARKERS INPUT. A negative polarity signal is required. Input impedance is 3 K in series with a silicon diode, with a sensitivity of about 0.2 V/db. A 1 V, 1 K signal source will cause at least a 1 db deflection on the display.
DRIFT CHARACTERISTICS	
With automatic balance:	Automatic balance system eliminates drift when operating with sweep oscillators having sweep speeds faster than 1 second. RF must be completely off during retrace.

Table 1-1. Tentative Specifications of the Model 8000/7051 Sweep Network Analyzer System (Cont.)

DRIFT CHARACTERISTICS (cont.)	
Without automatic balance:	When operating with single-frequency signals, with sweepers that do not have zero output during retrace, or at sweep speeds slower than 1 second, manual balance must be used. In this mode, drift will normally not exceed 3 db/hr. at -40 dbm in a normal laboratory environment. Drift is normally less than 1 db/hour above -30 dbm in all modes. A front panel manual balance adjustment allows correction for drift if necessary.
POWER REQUIREMENTS:	115/230 V, 50-400 Hz. Approximately 60 voltamperes. When operated at line frequencies from 65 to 400 Hz, manual balance must be used when calibrating.
MOUNTING DATA:	Removable cabinet sides permit rack-mounting.
DIMENSIONAL DATA:	Refer to the installation outline drawing, Figure 1-1.

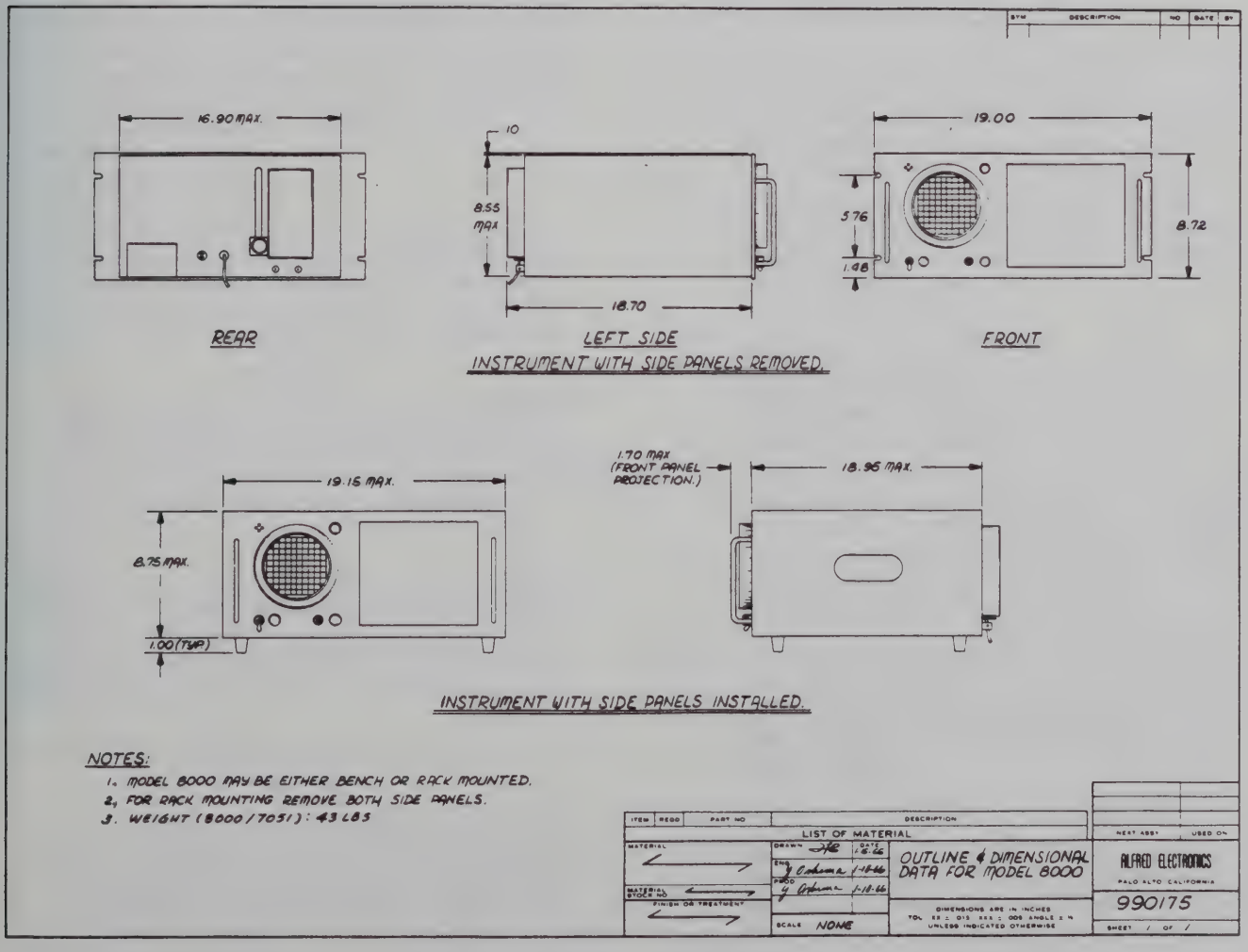


FIGURE 1-1. MODEL 8000/7051 INSTALLATION DRAWING

SECTION 2

INITIAL INSTRUCTIONS

2.1 RECEIVING INSPECTION.

Upon receiving your Model 8000/7051, carefully unpack the instrument and check for shipment damage. If some damage is evident, file a claim against the carrier. Refer to the Shipment Damage Claim form in the back of this manual.

2.2 SHIPPING SCREWS.

The Model 7051 Plug-in unit is secured to the Model 8000 Oscilloscope for shipping with two screws located underneath the unit at the points shown in Figure 5-2. They are used to prevent plug-in damage. Prior to regular use of the unit, these screws should be removed. They are easily identifiable by arrows marked on the bottom cover plate of the cabinet. The CRT tilt lever on the back of the instrument is secured in the bottom position to prevent movement of the CRT by means of a locking plate which hooks over the lever shaft and is secured by one screw, identified in Figure 3-2. Prior to regular use of the unit, remove the screw and take off the locking plate. Then re-install the screw.

2.3 POWER REQUIREMENTS.

The unit is normally connected at the factory for operation at 105 to 125 V ac (115 V ac nominal) and 50 to 400 Hz. However, provisions are provided for easy conversion to operation * at 210 to 250 V ac (230 V ac nominal). With the bottom cover removed, locate the power switch labeled 115 V AC (Figure 5-2). Remove the plate and move the switch forward to its alternate position. Turn the plate over and replace it with 230 V AC showing. To reconvert for 115 V ac operation, reverse the above procedure.

2.4 CHASSIS GROUNDING.

The instrument is supplied with a three-conductor power cord and a three-prong plug, which grounds the instrument when plugged into an appropriate receptacle. If a three-prong to two-prong adapter is used, make sure the unit is properly connected to ground by grounding the adapter pigtail lead.

WARNING

FAILURE TO PROPERLY GROUND THE INSTRUMENT CAN DEGRADE ITS PERFORMANCE AND STABILITY AND COULD ALLOW AN ABOVE-GROUND POTENTIAL TO BUILD UP ON THE CHASSIS, WHICH COULD BE DANGEROUS TO OPERATING PERSONNEL.

2.5 COOLING

Adequate space must be provided at the top, rear and bottom of the instrument for cooling purposes. Although this instrument does not require forced air cooling, due to use of all-solid-state components, proper ventilation for convection cooling is required, with one inch at the top and rear, and one-half inch at the bottom.

2.6 INCOMING INSPECTION TEST.

CAUTION

MANY INTERNAL ADJUSTMENTS LOCATED WITHIN THE MODEL 8000/7051 CHASSIS ARE CRITICAL. THEY HAVE BEEN CAREFULLY FACTORY-ADJUSTED PRIOR TO SHIPMENT AND SHOULD NOT NEED FIELD ADJUSTMENT. BECAUSE OF THE INTERACTION OF THESE ADJUSTMENTS A COMPLETE REALIGNMENT MAY BE REQUIRED IF THEY ARE DISTURBED. REFER TO SECTION 5 OF THIS MANUAL BEFORE TOUCHING ANY INTERNAL ADJUSTMENTS.

The following inspection test may be performed prior to regular operation of the Model 8000/7051. In each step, leave switch settings as made previously unless instructed otherwise.

2.6.1 DYNAMIC RANGE AND FUNCTIONAL PERFORMANCE CHECK.

a. Connect an ALFRED Model 1001 Crystal Detector (or equivalent) to the OUTPUT CALIBRATOR jack.

b. Connect the crystal detector output to the A CHN INPUT jack.

c. Make the following panel control settings:

POWER to ON
TRACE INTENSITY to mid-range for easy viewing
CALIBRATOR to -20 DBM
DISPLAY Mode Selector to CAL A CHN
DISPLAY BALANCE Control Switch to AUTO
VERTICAL SENSITIVITY (Both A Chn and B Chn) to 0.5 DB/DIV.
HORIZONTAL POSITION to mid-range

d. With the CALIBRATOR set at -20 DBM, and with the black A CHANNEL VERTICAL POSITION knob turned fully CCW out of the PRESET position, adjust the red knob to position the trace on the center horizontal line of the graticule.

e. Turn the black A CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to preset the digital counter readout to 20.0 DB LOSS. Then turn the black knob fully CCW, out of the PRESET position.

f. Switch the CALIBRATOR control to +10 DBM.

g. Turn the red A CHANNEL VERTICAL POSITION control CCW until the A CHANNEL GAIN DB digital counter reads 10.0 DB GAIN.

h. If the trace is not restored to the graticule centerline, note the trace position above or below the centerline. Then adjust the A CHN +10 CAL Screwdriver adjust control to position the trace the same amount in the opposite direction from the centerline, while the digital counter remains at the setting of step g.

i. If an adjustment was necessary in step h, a recheck must be made because of interaction between the +10 CAL adjustment and the initial trace position. Repeat steps d through h until no further adjustment is required in step h.

j. Switch the CALIBRATOR control to +20 DBM.

k. Turn the red A CHANNEL VERTICAL POSITION control CCW until the trace is again coincident with the graticule centerline. The A CHANNEL GAIN DB digital counter should read between 19.3 and 20.7.

* In Model 8000 instruments having S/N 391 and above, the 115 - 230 V power switch is located on the rear panel, rather than underneath the instrument. This switch is labeled in accordance with the factory voltage setting (normally 115 VAC) by means of a window in the escutcheon plate which holds the slide switch in the factory-set position. To convert to 230 V operation, remove the middle screw which retains the escutcheon plate, move the slide switch to the opposite position, and turn the escutcheon plate over for reattachment so that the 230 V lettering is visible.

l. Switch the CALIBRATOR control to 0 DBM.

m. Turn the red A CHANNEL VERTICAL POSITION control CW until the trace is again coincident with the graticule centerline. The A CHANNEL digital counter should read between 00.7 LOSS DB and 00.7 GAIN DB.

n. Switch the CALIBRATOR control to -10 DBM.

o. Turn the red A CHANNEL VERTICAL POSITION control CW until the trace is again coincident with the graticule centerline. The A CHANNEL LOSS DB digital counter should read between 9.3 and 10.7.

p. Switch the CALIBRATOR control to -30 DBM.

q. Turn the red A CHANNEL VERTICAL POSITION control CW until the trace is again coincident with the graticule centerline. The A CHANNEL LOSS DB digital counter should read between 29.3 and 30.7.

r. Switch the CALIBRATOR control to -40 DBM.

s. Turn the red A CHANNEL VERTICAL POSITION control CW until the trace is again coincident with the graticule centerline. The A CHANNEL LOSS DB digital counter should read between 39.3 and 40.7.

t. Connect the crystal detector output to the REF CHN INPUT jack and set the DISPLAY Mode Selector to CAL REF CHN.

u. Repeat steps d through g, except that digital counter GAIN and LOSS readings are interchanged because increasing power on the REF Channel requires LOSS Offset to restore the trace positions.

v. If the trace is not restored to the graticule centerline, note the trace position above or below the centerline. Then adjust the REF CHN +10 CAL Screwdriver adjust control to position the trace the same amount in the opposite direction from the centerline, while the digital counter remains at the setting of step g.

w. If an adjustment was necessary in step v, a recheck must be made because of interaction between the +10 CAL adjustment and the initial trace position. Repeat steps d through g and v until no further adjustment is required in step v.

x. Repeat steps j through s, except that digital counter GAIN and LOSS readings are interchanged.

y. Connect the crystal detector output to the B CHN INPUT jack and set the DISPLAY Mode Selector to CAL B CHN.

z. Repeat steps d through g, except use the B CHANNEL VERTICAL POSITION control knobs and digital indicators.

aa. If the trace is not restored to the graticule centerline, note the trace position above or below the centerline. Then adjust the B CHN +10 CAL Screwdriver adjust control to position the trace the same amount in the opposite direction from the centerline, while the digital counter remains at the setting of step g.

bb. If an adjustment was necessary in step aa, a recheck must be made because of interaction between the +10 CAL adjustment and the initial trace position. Repeat steps d through g and aa, until no further adjustment is required in step aa.

cc. Repeat steps j through s, except use the B CHANNEL VERTICAL POSITION control knobs and digital indicators.

2.6.2 STABILITY CHECK.

NOTE: This check applies to instruments above Serial No. 20. On instruments below Serial No. 20, use the LOG position in steps c and h (with internal sweep); and conclude the test with step i.

a. Leave connections and control settings as in the final step of Paragraph 2.6.1 above, except for the following changes in control settings:

DISPLAY Mode Selector to BAL B CHN
CALIBRATOR Control to OFF

b. Adjust the B CHN BALANCE Screwdriver control if necessary to position the trace exactly on the graticule centerline.

c. Make the following changes in control settings:

DISPLAY Mode Selector to CAL B CHN
CALIBRATOR Control to -40 DBM

d. Switch the DISPLAY BALANCE control back and forth between MANUAL and AUTO. There should be no noticeable movement in the trace position.

e. Connect the crystal detector output to the A CHN INPUT jack.

f. Make the following changes in control settings:

DISPLAY Mode Selector to BAL A CHN
CALIBRATOR Control to OFF

g. Adjust the A CHN BALANCE Screwdriver control if necessary to position the trace exactly on the graticule centerline.

h. Make the following changes in control settings:

DISPLAY Mode Selector to CAL A CHN
CALIBRATOR Control to -40 DBM

i. Switch the DISPLAY BALANCE control back and forth between MANUAL and AUTO. There should be no noticeable movement in the trace position.

j. Connect the crystal detector output to the REF CHN INPUT jack.

k. Make the following changes in control settings:

DISPLAY Mode Selector to BAL REF CHN
CALIBRATOR Control to OFF

l. Adjust the REF CHN BALANCE Screwdriver control if necessary to position the trace exactly on the graticule centerline.

m. Make the following changes in control settings:

DISPLAY Mode Selector to CAL REF CHN
CALIBRATOR Control to -40 DBM

n. Switch the DISPLAY BALANCE control back and forth between MANUAL and AUTO. There should be no noticeable movement in the trace position.

2.6.3 CRT DISPLAY CALIBRATION CHECK.

a. Connect the crystal detector to the OUTPUT CALIBRATOR jack.

b. Connect the crystal detector output to the A CHN INPUT jack.

NOTE: Be sure that the A CHN BAL and +10 CAL adjustments have been properly adjusted as in paragraphs 2.6.1 and 2.6.2 above.

c. Make the following changes in control settings:

CALIBRATOR to -10 DBM
DISPLAY Mode Selector to LOG A CHN
DISPLAY BALANCE to AUTO
A CHN VERTICAL SENSITIVITY to 0.5 DB/DIV
HORIZONTAL POSITION SENSITIVITY to INTERNAL SWEEP

d. Adjust the red A CHANNEL VERTICAL POSITION knob to move the trace to the centerline on the graticule. Turn the black A CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to preset the digital counter readout to 00.0 DB. Then turn the black knob fully CCW, out of the PRESET position. Then change the A CHN VERTICAL SENSITIVITY setting to 10 DB/DIV.

e. Turn the red A CHANNEL VERTICAL POSITION knob CW until the digital counter reads 50.0 DB LOSS. The trace should shift to within ± 2 mm of the top graticule line.

f. Turn the red A CHANNEL VERTICAL POSITION knob CCW until the digital counter reads 50.0 DB GAIN. The trace should shift to within ± 2 mm of the bottom graticule line.

g. Set the A CHN VERTICAL SENSITIVITY control to 5 DB/DIV.

h. Turn the red A CHANNEL VERTICAL POSITION knob CW until the digital counter reads 25.0 DB GAIN. The trace should shift to within ± 2 mm of the bottom graticule line.

i. Turn the red A CHANNEL VERTICAL POSITION knob CW until the digital counter reads 25.0 DB LOSS. The trace should shift to within ± 2 mm of the top graticule line.

j. Set the A CHN VERTICAL SENSITIVITY control to 2 DB/DIV.

k. Turn the red A CHANNEL VERTICAL POSITION knob CCW until the digital counter reads 10.0 DB LOSS. The trace should shift to within ± 2 mm of the top graticule line.

l. Turn the red A CHANNEL VERTICAL POSITION knob CCW until the digital counter reads 10.0 DB GAIN. The trace should shift to within ± 2 mm of the bottom graticule line.

m. Set the A CHN VERTICAL SENSITIVITY control to 1 DB/DIV.

n. Turn the red A CHANNEL VERTICAL POSITION knob CW until the digital counter reads 5.0 DB GAIN. The trace should shift to within ± 2 mm of the bottom graticule line.

o. Turn the red A CHANNEL VERTICAL POSITION knob CW until the digital counter reads 5.0 DB LOSS. The trace should shift to within ± 2 mm of the top graticule line.

p. Set the A CHN VERTICAL SENSITIVITY control to 0.5 DB/DIV.

q. Turn the red A CHANNEL VERTICAL POSITION knob CCW until the digital counter reads 2.5 DB LOSS. The trace should shift to within ± 2 mm of the top graticule line.

r. Turn the red A CHANNEL VERTICAL POSITION knob CCW until the digital counter reads 2.5 DB GAIN. The trace should shift to within ± 2 mm of the bottom graticule line.

s. Repeat steps b through r with the crystal detector output connected to the B CHN INPUT jack and using B Channel control settings.

NOTE: If performance in the above tests is outside the specified limits, refer to the trouble-shooting and adjustment procedures in Section 5 of this manual.

2.7 RETURNING THE INSTRUMENT.

If it becomes necessary to return the instrument to ALFRED ELECTRONICS, authorization must first be obtained from our Sales Department.

When authorization is received, prepare the instrument for shipment by securing the plug-in unit in the Model 8000 with two shipping screws installed through the holes marked by arrows in the bottom of the cabinet. The CRT tilt lever on the back of the instrument should be moved to the bottom position, tightened, and secured by means of the locking plate shipped with the instrument. This locking plate hooks over the lever shaft and is secured by one screw, identified in Figure 3-2. A protective shipping plate or a piece of cardboard should be placed over the CRT graticule area for protection. A board or heavy cardboard buffer should be placed in front of the unit across the handles to protect the panel from blows against the container.

The instrument should be wrapped in a protective material such as polyethylene and heavy wrapping paper to protect against marring by the padding used in the container. A sufficient quantity of padding material, such as hair flex, should be placed all around the instrument for cushioning. If the original shipping container is not available, an equivalent rugged cardboard container or wooden crate should be used for the packing carton. Pack the instrument so that it cannot move around in the container. A letter containing all pertinent information should be included in the package, unless such a letter has previously been sent to our Sales Department.

SECTION 3 - OPERATION

3.1 FRONT PANEL CONTROLS (See Figure 3-1).

A functional description of all front panel controls is given in Table 3-1. In the table, CW and CCW are used to abbreviate clockwise anc

3.2 FRONT PANEL CONNECTORS (See Figure 3-1).

A functional description of all front panel connectors is given in Table 3-2.

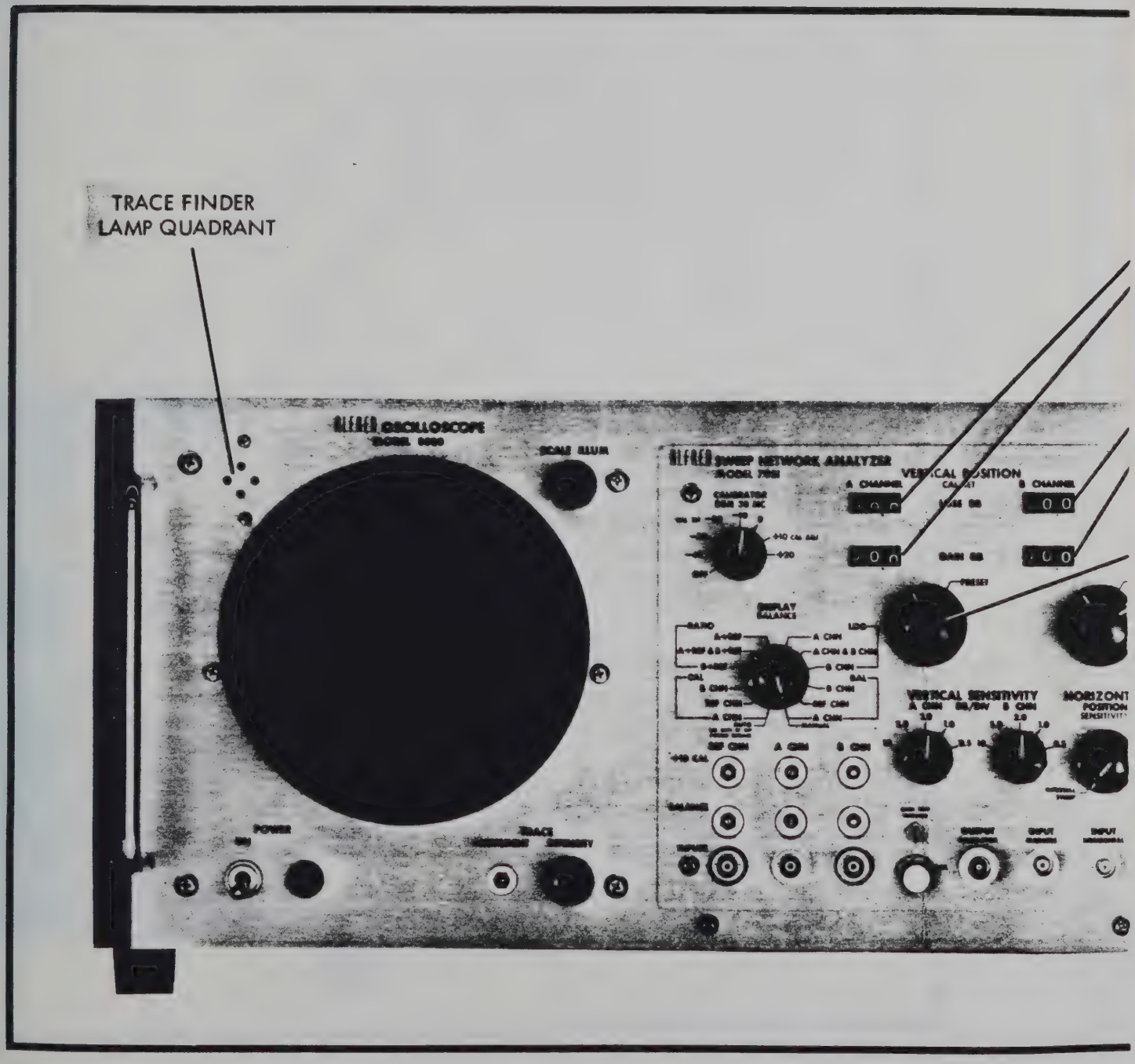
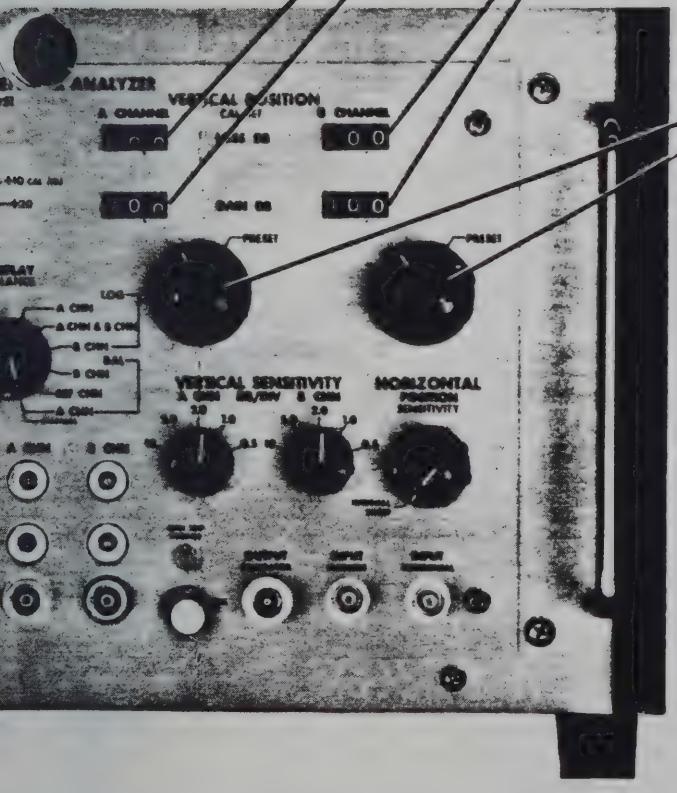


FIGURE 3-1. FRONT PANEL

nd CCW are used to abbreviate clockwise and counter-clockwise, respectively.



DIGITAL COUNTERS (INDICATING RANGE IS 00.0 TO 99.9 DB GAIN OR LOSS; DYNAMIC RANGE WITH VERTICAL POSITION OFFSET ADJUSTMENT IS 60 DB OF GAIN OR LOSS

RED KNOB ADJUSTS VERTICAL POSITION OFFSET (MONITORED BY DIGITAL COUNTERS) WHEN BLACK KNOB IS FULLY CCW; AND PRESETS THE DIGITAL COUNTERS WITHOUT AFFECTING OFFSET WHEN BLACK KNOB IS TURNED TO PRESET POSITION

INCREASES LOSS OFFSET (MOVES TRACE UP)

INCREASES GAIN OFFSET (MOVES TRACE DOWN)

CAUTION
TO AVOID EXCESSIVE WEAR ON DIGITAL COUNTERS, DO NOT EXCEED 15 DB/SECOND ADJUSTMENT SPEED

GURE 3-1. FRONT PANEL

Table 3-1. Description of Front Panel Controls and Indicators

Control or Indicator	Function
CALIBRATOR DBM 30 MC Control	Controls the output level of the 30 mc rf calibration signal supplied at the OUTPUT CALIBRATOR jack. In the OFF position, turns off the solid-state calibration oscillator and disconnects the OUTPUT CALIBRATOR jack from the calibration oscillator circuit. In other positions, supplies a calibrated output signal level equivalent to the switch position label, –40 DBM to +20 DBM. Output accuracy is ± 0.3 DB at + 20 DBM. Accuracy of the attenuator, which reduces the output level for outputs below +20 DBM, is ±0.3 DB.
VERTICAL POSITION Offset Controls	Separate, independent controls are provided for the A and B channels. When the black concentric knob is CCW, out of the PRESET position, the red knob adjusts an offset control potentiometer that supplies up to 60 db gain or loss offset in the display circuit. The gain or loss offset is indicated directly on the GAIN or LOSS DB 3-digit counters. Turning the red knob CW changes the offset in the direction of increasing loss (moves trace upward); turning it CCW changes the offset in the direction of increasing gain (moves trace downward). Gain offset has the effect of moving the display down on the CRT graticule; loss offset moves the display up on the CRT graticule. The amount of offset is given by the db reading shown in the GAIN DB or LOSS DB windows. When the black concentric knob is turned CW to the PRESET position, the red knob is disengaged from the offset potentiometer. It thus no longer adjusts the display position offset, but still operates the 3-digit counter mechanism. This PRESET mode permits setting the counter to any desired calibration reading after the display has been moved to the desired calibration position on the graticule with the black knob CCW (out of the PRESET position). A typical operating sequence is as follows: With the black knob CCW (out of the PRESET position), set the calibration trace (known signal level or ratio) on the CRT graticule centerline by turning the red knob. Then turn the black knob CW to the PRESET position and use the red knob to set the digital indicator to the calibration reading (corresponding to the known signal level or ratio). Turn the black knob CCW and the instrument is ready for measurement operations. Now, when the red knob is turned to restore any point of the displayed signal to the graticule centerline, the signal level or ratio at that point on the display is given directly in dbm or db by the GAIN DB or LOSS DB indicators. To measure the db variation between any two points on the display, move each point to the centerline in turn, and note the difference between the two digital counter readings obtained.
VERTICAL POSITION GAIN DB and LOSS DB Counter-Indicators	Indicate the gain or loss offset provided by the VERTICAL POSITION Offset Controls, with 0.1 db resolution. Range is from 00.0 to ± 60.0 db. These indicators can be used for direct digital readout of db ratios or dbm power levels, after the VERTICAL POSITION Offset Controls have been used to return a performance trace to the calibrated (zero-set) graticule position.
DISPLAY Mode Selector switch	Controls the operating mode of the instrument. In the RATIO positions, the CRT display measures the ratio of one or two input signals with respect to a third (reference) signal, directly in db. In the LOG positions, the CRT display measures the absolute level of one or two input signals, in dbm. In the CAL positions, with the internal rf calibrator supplying a drive signal to each detector, the instrument displays the output of each channel individually. This allows a calibration adjustment of each logarithmic converter amplifier to compensate the detector crystal driving each channel. In the BAL positions, the instrument displays the balance of each channel individually to allow manual balancing of the low-level input stages.
BALANCE Mode Selector (red)	Concentric with the DISPLAY Mode Selector; controls the balancing mode of the instrument. Selects automatic or manual rebalancing. In the AUTO mode, the swept rf signal driving the test loop must be operated in a "retrace off" mode (i.e., rf turned completely off during retrace), and the effect of drift in the low level input stages is eliminated. For operation with single-frequency signals or with swept signals that remain on during retrace, the MANUAL mode must be used. The excellent circuit stability eliminates the need for frequent manual rebalancing in the MANUAL mode.
VERTICAL SENSITIVITY Selector switch	Separate, independent controls are provided for the A and B channels. These controls permit the display sensitivity to be adjusted from 10 DB/DIV to 0.5 DB/DIV in 5 steps. With suitable control settings the CRT graticule scale provides direct db readout of ratio measurements, or direct dbm readout of absolute measurements.

Table 3-1. Description of Front Panel Controls and Indicators (Cont.)

Control or Indicator	Function
HORIZONTAL POSITION control.	Adjusts the horizontal position of the trace on the CRT, and allows convenient centering of the 10-cm display. Normally used to set the left-hand limit of the horizontal sweep at a point 5 cm left of center.
SENSITIVITY Control (red)	Concentric with the HORIZONTAL POSITION control; adjusts horizontal display for full scale deflection with sweep signal inputs to the INPUT HORIZONTAL jack ranging from 10 to 50 V. When turned fully CW, provides maximum gain. Normally used to set the right-hand limit of the horizontal sweep at a point 5 cm right of center after the left-hand limit has been set by the HORIZONTAL position control. When turned fully CCW to the INTERNAL SWEEP switched position, disables the INPUT HORIZONTAL jack and connects the internal sweep generator to spread the CRT presentation.
+10 CAL Screwdriver adjustment	Separate, independent controls are provided for the REF, A, and B Channels. These controls permit calibration of each log converter amplifier to compensate the crystal detector driving that channel. The +10 CAL adjustment is made to achieve tracking of the detector amplifier response with the calibrator output over the transition range between -20 dbm and +10 dbm. By thus adjusting the internal compensation circuitry to match the square law deviation of the crystal, the instrument is calibrated for direct db readout over the full useful range of the crystal (from -40 to about +20 dbm).
BALANCE Screwdriver adjustment	Separate, independent controls are provided for the REF, A, and B Channels. These controls permit manual balancing of the low-level differential input stage of each amplifier to eliminate build-up of drift potential, when the operating mode will not permit automatic balancing.
OVEN TEMP STABILIZED Indicator light	Glows when the temperature-regulated circuits have stabilized.
Cathode Ray Tube (CRT)	Provides a single-channel or chopped dual-channel readout presentation, depending upon the setting of the DISPLAY Mode Selector switch. When used for swept-frequency measurements, the CRT presentation is a db plot of the measured function(s) vs frequency. When used for single-frequency measurements, the CRT presentation is a horizontal line whose vertical position is a function of the quantity being measured.
SCALE ILLUM Control	Controls the illumination of the graticule lines in front of the CRT screen. Increases the illumination when turned CW; eliminates it when turned fully CCW.
TRACE INTENSITY Control	Controls the intensity of the CRT trace. Brightens the trace when turned CW.
TRACE ALIGNMENT Screwdriver adjustment	Permits tilting a horizontal trace to allow exact horizontal alignment of the trace with the graticule lines. Useful when instrument is in the vicinity of magnetic devices which may tilt the trace.
TRACE FINDER Lamp quadrant (at upper left of CRT)	When trace goes off scale in any direction, the corresponding lamp will glow to aid in determining the proper adjustment to restore the trace to the face of the CRT.
POWER Switch	Applies power to the 8000/7051 when in the ON position. Removes all power when turned off.
POWER Indicator light	Glows when power is applied to the instrument.

Table 3-2. Description of Front Panel Connectors.

Control or Indicator	Function
INPUTS	Separate isolated BNC jacks are provided for the Reference, A, and B Channels, to receive the input signals from the crystal detectors in the test circuit. The insulators which isolate the jacks from the panel are color-coded. Connections and detectors can be similarly color-coded for ease of channel identification, if desired.
OUTPUT CALIBRATOR	Supplies the 30-MHz calibration signal output, at the level set on the CALIBRATOR control, for use in detector calibration.
INPUT MARKERS	Accepts video marker pulses for display on the CRT presentation to calibrate the horizontal axis in frequency. A negative polarity signal is required. A 1 V, 1 K signal source will cause at least a 1-db pip on the display.
INPUT HORIZONTAL	Accepts a horizontal sweep drive signal from the rf sweep generator to sweep the CRT display in synchronism with the frequency sweep. Inputs ranging from 10 to 50 volts can be adjusted to provide full-width sweeps with a proper setting of the HORIZONTAL POSITION SENSITIVITY control. Input impedance is about 100 K ohms.

3.3 REAR PANEL CONTROLS AND CONNECTORS (See Figure 3-2). A functional description of all rear panel controls and connectors is given in Table 3-3.

Table 3-3. Description of Rear Panel Controls and Connectors.

Control or Indicator	Function
CRT face tilt knob	Operates in a vertical slot to permit tilting the face of the CRT to a plane perpendicular to the sight angle.
REC VERT jack	Supplies a dc output signal for driving the Y axis of an external recorder. The output level is linear in db, proportional to the instantaneous vertical signal applied to the CRT, with a sensitivity of about 0.2 V per cm of vertical CRT deflection. Output impedance is 10 K.
REC HORIZ jack	Supplies a dc output signal for driving the X axis of an external recorder. The output level is proportional to the instantaneous horizontal signal applied to the CRT, with a sensitivity of about 0.2 V per cm of horizontal CRT deflection. Output impedance is 10 K.
LINE FUSE F_1	This 2-amp slow-blow fuse provides primary power protection for the instrument. All line power passes through this fuse.

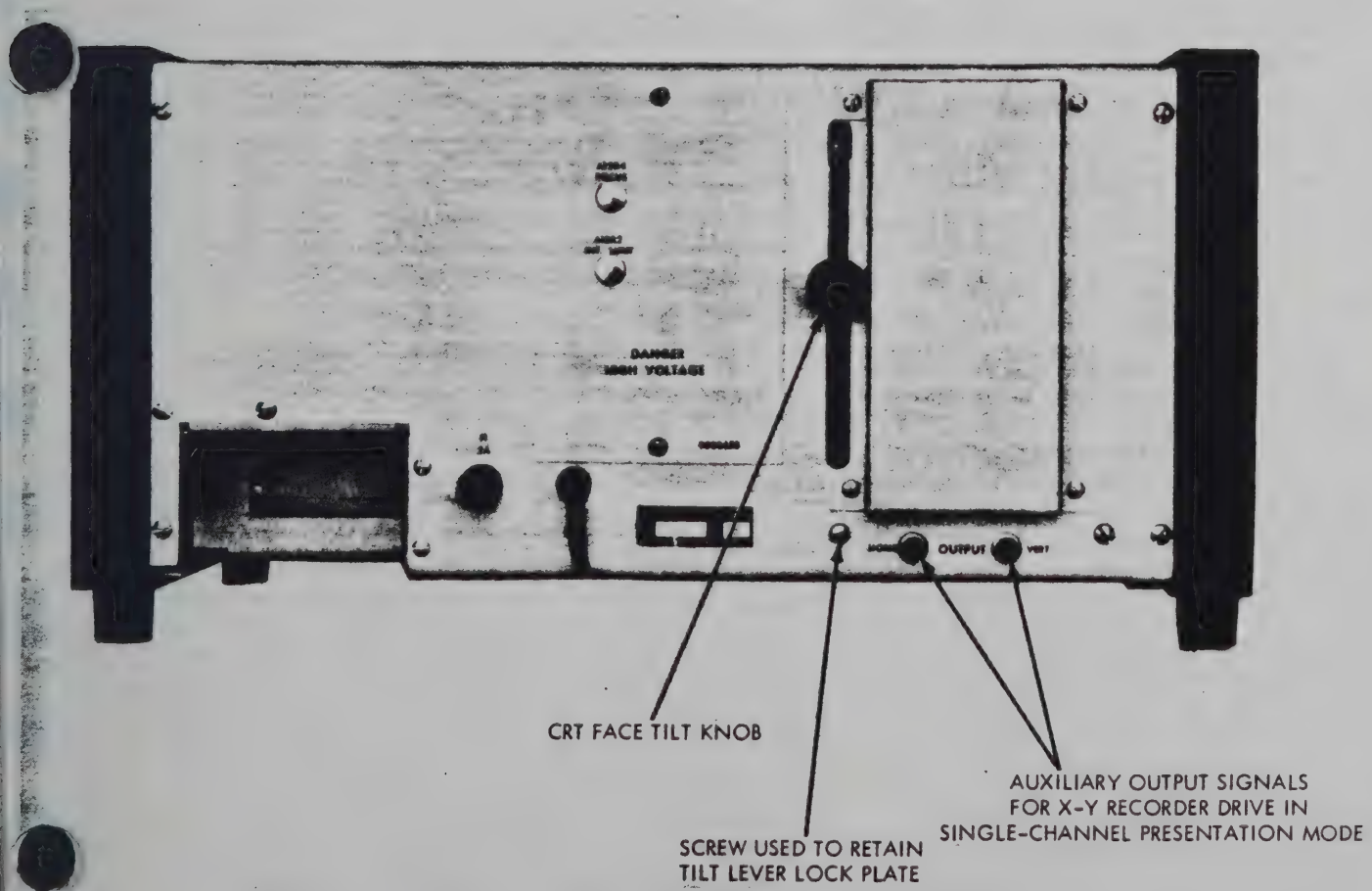

CRT FACE TILT KNOB
SCREW USED TO RETAIN TILT LEVER LOCK PLATE
AUXILIARY OUTPUT SIGNALS FOR X-Y RECORDER DRIVE IN SINGLE-CHANNEL PRESENTATION MODE

FIGURE 3-2. REAR PANEL

3.4 INSTRUMENT TURN-ON PROCEDURE.

a. Check that the line cord is plugged in and properly grounded.

b. Check that the Model 7051 Plug-in unit is securely locked in position in the Model 8000 Oscilloscope, with the LOCK knob tightened.

c. Check that the TRACE INTENSITY control is in a mid-range position, not the fully CW position (which would shorten CRT life by making the trace too bright).

d. Turn the POWER toggle switch ON.

e. The POWER ON indicator light should glow immediately. If not, check the line fuse F1 on the rear panel.

f. Set the DISPLAY Mode Selector switch to LOG A CHN, set the CALIBRATOR control to 0 DBM, and set the A CHN VERTICAL SENSITIVITY to 10 DB/DIV.

g. Connect a crystal detector to the OUTPUT CALIBRATOR jack, and connect the detector output to the A CHN INPUT jack.

h. After about 5 minutes, the OVEN TEMP STABILIZED light should glow. The instrument is now ready for measurement operations.

i. Adjust the TRACE INTENSITY control to achieve the desired trace brilliancy on the CRT.

j. Turn the red HORIZONTAL POSITION SENSITIVITY control fully CW to the INTERNAL SWEEP position. Adjust the HORIZONTAL POSITION control as necessary to center the trace on the CRT, and check that the trace is parallel with the horizontal graticule lines. If not, adjust the TRACE ALIGNMENT screwdriver adjustment as necessary to achieve the proper horizontal alignment.

k. Turn the SCALE ILLUM control to the setting that provides the desired amount of graticule illumination.

l. If the instrument has not been calibrated for the detectors to be used for each channel, carry out the necessary calibration using the procedure of Paragraph 3.5.

m. Turn to the appropriate paragraph(s) below for the control settings and operating procedures for the desired mode of operation.

CAUTION

Do not remove the plug-in unit (Model 7051) from the Model 8000 or re-install it when the Model 8000 POWER switch is ON.

3.5 DETECTOR COMPENSATION CALIBRATION PROCEDURE (See Figure 3-3).

NOTE: Most standard crystal detectors can be used with the Model 8000/7051, provided the video impedance of the crystal (at -30 dbm) is less than 20 K. All current production ALFRED Model 1001 Crystal Detectors satisfy this requirement. The simplest test of whether a crystal detector is suitable or not is to perform the calibration procedure below. If the crystal can be calibrated in accordance with this procedure, and then will drive the Model 8000/7051 so that its calibrated readout "tracks" the CALIBRATOR Switch setting over its full range, the crystal is satisfactory. To assure performance which meets published specifications (Table 1-1) from 10 MHz to 8.0 GHz, and approximates these specifications to 12.4 GHz, the ALFRED Model 1403 Crystal Detector Set is available. This set consists of three Model 1001 Crystal Detectors which are checked for proper operation with the Model 8000/7051, plus three interconnecting cables terminated in BNC Connectors.

Once a particular channel of the Model 7051 is calibrated to compensate for the non-square-law performance of a given detector, thereby establishing an accurate square-law transducer channel with a 60-db dynamic range, it will not be necessary to re-calibrate as long as the same detector or sampler is used to drive the same channel, and as long as the temperature environment remains reasonably constant. Therefore, the detector or samplers should be labeled and always used to drive the same channel where possible, to cut down the amount of detector compensation calibration required. The color-coded INPUT jack insulators can be used for a color-coded labeling scheme.

Note that detector compensation calibration converts the combination of the detector and the Model 7051 into a 60-db range logarithmic transducer. Since the VERTICAL POSITION Indicator digital counter settings used in calibration are equal to the calibration power levels, this calibration adjusts the VERTICAL POSITION Indicator digital counters to provide direct readout of dbm levels between -40 and +20 dbm, thereby making the instrument a swept power meter.

After calibration is performed, when RATIO measurements are made, the VERTICAL POSITION Indicator digital counters may be preset to different readings, as directed in the ratio measurement procedure, to provide proper zero-set in a ratio measurement test set-up. This will not affect the 60-db-range logarithmic calibration, but will mean that the instrument no longer reads absolute level in dbm. For this reason a simplified power level readout calibration procedure is given in Paragraph 3.8.2 to permit resetting the VERTICAL POSITION Indicator digital counters to read directly in dbm whenever absolute power readout is desired, without repeating the full logarithmic calibration procedure given below.

Note that detector compensation calibration is theoretically a function of temperature, and thus should be checked periodically in a changing environment. In a normal lab environment with a nearly constant temperature, recalibration is rarely necessary once the instrument is up to operating temperature. In order to reduce temperature fluctuations, it is best to leave the instrument turned on all day if it is to be used frequently.

a. Turn the instrument on as directed in Paragraph 3.4, and make the following control settings:

CALIBRATOR Control to -20 DBM
DISPLAY Mode Selector to CAL B CHN
DISPLAY BALANCE Control switch to AUTO
VERTICAL SENSITIVITY (Both A CHN and B CHN) to 10 DB/DIV

b. Connect the output jack of the detector(s) to be used in the subsequent measurement procedures, to the proper INPUTS jacks (REF CHN, A CHN, or B CHN) on the Model 7051 front panel. Follow the Model 1403 detector color-coding scheme, i.e. blue to REF channel, yellow to A channel, and orange to B channel. If other than Model 1403 detectors are used, label these detector(s) and sampler(s) as to channel, so that once they are calibrated, they can be retained with the same channel.

NOTE: The following procedure is set up to calibrate the channels in the order B, REF, A. The REF channel must be calibrated before the A channel to preserve the A channel digital counter calibration in terms of absolute power. Doing the B channel first provides familiarization with the procedure before experiencing the inversion which takes place when calibrating the REF channel.

c. Connect the rf input terminal of the Channel B crystal detector to the Model 7051 OUTPUT CALIBRATOR jack, using suitable rf connecting hardware.

NOTE: If a sampler or waveguide detector, rather than a simple coaxial detector, is being used to drive the channel under test, the detector must be removed from the sampler for direct connection to the OUTPUT CALIBRATOR signal. If this is not possible, a known-level signal at a frequency within the sampler passband must be used to drive the detector through the sampler or waveguide input port, with a level sufficient to apply first -20 dbm and then +10 dbm to the detector. Since this external calibrator signal will not be modulated to be "off" during the internal sweep retrace, set the DISPLAY BALANCE switch to MANUAL and check the manual balance as directed in Paragraph 3.7.

d. Turn the red B CHANNEL VERTICAL POSITION knob to set the trace on the first horizontal line below the graticule centerline.

e. Switch the CALIBRATOR control to +10 DBM.

f. The trace should be shifted to the second horizontal line above the graticule centerline, making a step of 3 scale divisions in response to the 30-db increase in power. If the actual shift is greater or less than 3 scale divisions, note the amount and direction of this position error.

g. Adjust the B CHN +10 CAL Screwdriver Adjust control to move the trace to the desired line, and then cross the line to a final position on the opposite side of the desired line from step f, and 1.5 times as far from the desired line. (Moving the trace seemingly farther away on the opposite side of the desired position actually helps converge the calibration process because it compensates for the effect of the adjustment on the low-power display.)

h. Switch the CALIBRATOR control to -20 DBM.

i. Repeat steps d through h.

j. Switch the B CHN VERTICAL SENSITIVITY to 0.5 DB/DIV.

k. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW out of the PRESET position, adjust the red knob to position the trace on the center horizontal line of the graticule.

l. Turn the black B CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to set the digital counter readout to 20 DB LOSS. Then turn the black knob fully CCW, out of the PRESET position.

m. Switch the CALIBRATOR control to +10 DBM.

n. Turn the red B CHANNEL VERTICAL POSITION control CCW until the A CHANNEL GAIN DB digital counter reads 10 DB GAIN.

o. If the trace is not restored to the graticule centerline, note the trace position above or below the centerline. Then adjust the B CHN +10 CAL Screwdriver adjust control to position the trace the same amount in the opposite direction from the centerline, while the digital counter remains at the setting of step n.

p. If an adjustment was necessary in step o, a recheck must be made because of interaction between the +10 CAL adjustment and the initial trace position. Repeat steps k through o until no further adjustment is required in step o.

q. Connect the rf input terminal of the Channel REF crystal detector to the Model 7051 OUTPUT CALIBRATOR jack, using suitable rf connecting hardware.

r. Make the following changes in switch settings:
CALIBRATOR Control to -20 DBM
DISPLAY Mode Selector to CAL REF CHN
A CHN VERTICAL SENSITIVITY to 10 DB/DIV

s. Repeat steps d through p to calibrate the REF Channel. Note that in the calibration mode, the REF Channel uses the Channel A electronics and controls. Thus, the CHANNEL A VERTICAL POSITION and SENSITIVITY controls and digital counter should be substituted in the procedure. Due to the automatic inversion applied to the REF Channel, increasing power moves the trace down. Therefore, in step d set the trace on the first horizontal line above the graticule centerline and look for a downward shift as power is increased. In step n, use 30 DB additional LOSS offset (for a setting of 50 DB LOSS) rather than GAIN offset.

t. Connect the rf input terminal of the Channel A crystal detector to the Model 7051 OUTPUT CALIBRATOR jack, using suitable rf connecting hardware.

u. Make the following changes in switch settings:
CALIBRATOR Control to -20 DBM
DISPLAY Mode Selector to CAL A CHN
A CHN VERTICAL SENSITIVITY to 10 DB/DIV

v. Repeat steps d through p, substituting the CHANNEL A VERTICAL POSITION and SENSITIVITY controls and digital counter.

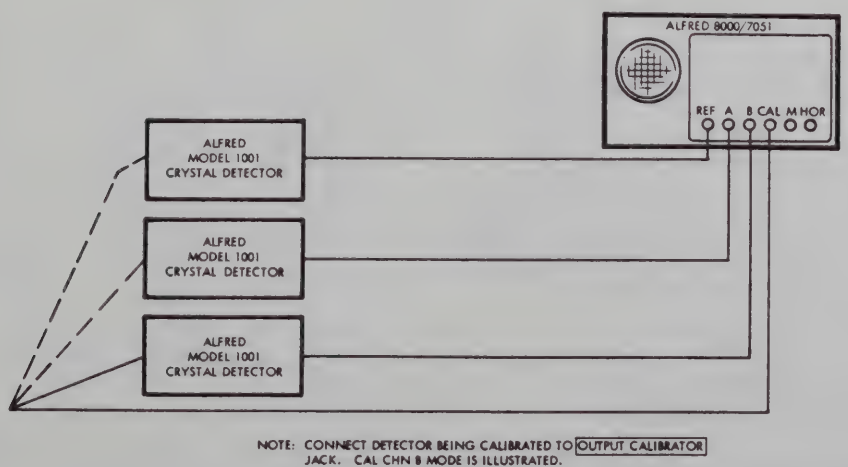


FIGURE 3-3 CONNECTIONS FOR DETECTOR CALIBRATION

3.6 DISCUSSION OF ALTERNATE READOUT METHODS.

3.6.1 GENERAL. The Model 8000/7051 provides direct readout for either channel individually or both channels simultaneously, from the CRT and digital counters. In addition it provides auxiliary output signals suitable for driving an external X-Y recorder when in the single-channel presentation mode. The CRT readout mode permits "at-a-glance" readout, while the digital counters provide high-accuracy readout with 0.1 db resolution. The X-Y recorder drive or an oscilloscope camera can be used for permanent recording of the display. Each of these readout methods is discussed in more detail below.

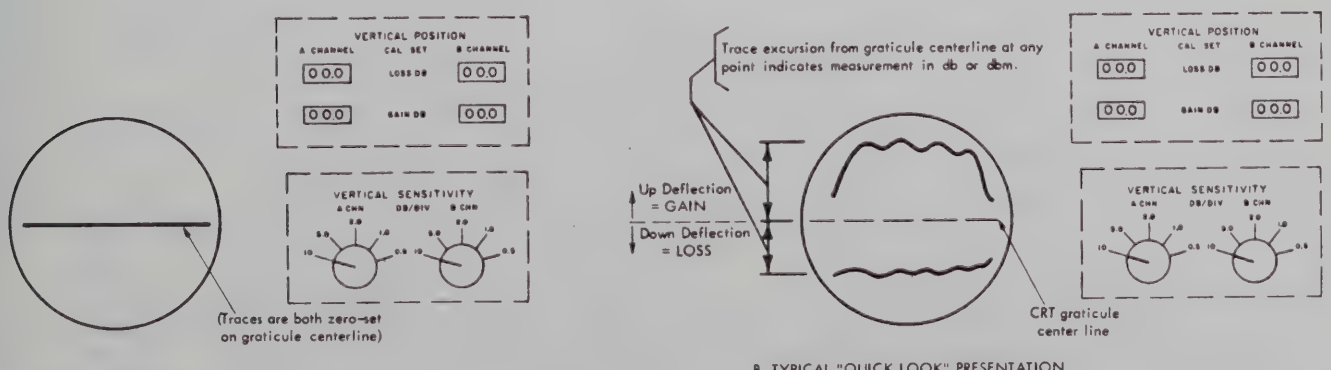
3.6.2 CRT DISPLAY READOUT. In this mode, each trace is zero-set to the graticule centerline with the VERTICAL POSITION Controls. For measurements, a VERTICAL SENSITIVITY control setting is used that gives on-scale presentation of all trace excursions over the swept band of interest. Typical zero-set and performance trace displays are shown in Figure 3-4. The presentation is a typical plot of amplitude (vertical axis) vs. frequency (horizontal axis), and the signal deviation from the zero-set level can be measured by "counting squares" vertically between the zero-set line and the trace position at any point. Frequency points on the horizontal axis can be identified by applying video markers to the INPUT MARKERS jack, or by evaluating horizontal position in terms of the frequency sweep ramp signal being supplied to the INPUT HORIZONTAL jack.

NOTE. If video markers are to be applied to the INPUT MARKERS jack, the maximum sweep speed used should be limited to 100 ms (0.1 sec minimum sweep time) to avoid loss or attenuation of the marker pips due to frequency response limitations.

To achieve a high-sensitivity CRT display, calibrated electronic offset may be used to balance out the signal amplitude to return the trace to the graticule centerline at an average or limiting value. This capability of the VERTICAL POSITION controls permits display of trace variations with greater resolution than would otherwise be possible, and eliminates the need for external variable attenuators or amplifiers to restore the measured level to the zero-set level as in "standard" test procedures. For example, Figure 3-5 illustrates use of offset to "cancel out" the minimum gain of a leveled amplifier to enable examination of the level variations at the highest sensitivity setting. If the highest sensitivity setting were used without offset, the trace would be driven off scale from the zero-set line. Note that signal variations between points on the display may be read from the calibrated CRT without zero-set lines. Note also that use of internal electronic offset instead of external variable attenuators provides greater flexibility by allowing any level of operation to be offset for CRT examination, without attenuating the rf signal level at the detector. One of the inherent advantages of a logarithmic display is that a 1-db variation produces the same deflection on the CRT regardless of the offset signal level.

NOTE: The characteristic shape of each trace (or the response of a particular trace to slight adjustment of the corresponding VERTICAL POSITION control) normally permits simple identification of each trace in the dual CRT display. It is possible to zero-set each trace to different graticule lines, such as 2 cm above and 2 cm below the graticule centerline, to obtain trace separation. In that case, the VERTICAL SENSITIVITY control must be left in the setting used for zero-set adjustment, because when the display is zero-set to any line except the graticule centerline, the zero-set Offset adjustment does not null out the zero-set signal level, and the offset to the non-centered zero-set position will change when the VERTICAL SENSITIVITY control setting is changed.

3.6.3 DIGITAL COUNTER READOUT. This method measures a signal deviation by comparing the deviation with the precision internal offset which is calibrated directly in db. The precision offset is used to return any desired point of measurement on the performance trace to the graticule centerline, the point where 0 vertical deflection signal is generated, so that any non-linearities or other inaccuracies of the summing amplifiers, chopper amplifiers, deflection amplifiers, and CRT are eliminated from the measurement. This measurement mode, illustrated in Figure 3-6, provides the greatest accuracy. In this mode, each trace is zero-set to the graticule centerline by means of the VERTICAL POSITION controls. The highest VERTICAL SENSITIVITY setting should be used. For measurements, the VERTICAL POSITION controls are used to restore the points of interest on the waveform exactly to the graticule centerline. The measured value of each trace at the zero-line crossing can then be read directly in db or dbm, with 0.1 db resolution, from the VERTICAL POSITION GAIN DB or LOSS DB digital counters.



A. TYPICAL ZERO-SET DISPLAY

B. TYPICAL "QUICK LOOK" PRESENTATION FOR CRT READOUT DIRECTLY FROM SELF-CALIBRATED GRATICULE.

FIGURE 3.4 TYPICAL "QUICK-LOOK" OR GO/NO-GO" READOUT DIRECTLY FROM CALIBRATED CRT

3.6.4 X-Y RECORDER READOUT. This mode can be used only with single-channel settings of the DISPLAY switch, because the chopping rate (100 KHz) used for the dual-channel presentations is well above the frequency response range of X-Y recorders. To obtain an X-Y recording, lift the recorder pen and then connect the rear panel REC VERT jack to the recorder Y axis, and the REC HORIZ jack to the recorder X axis.

For recording swept measurements place the rf signal source in the triggered, single-sweep mode. This requires the Model 7051 BALANCE switch to be in the MANUAL position. The manual balance of each channel should be checked in accordance with paragraph 3.7.3 before beginning measurement operations. Make a "dry run" with the recorder pen lifted to check recorder range and settings. Then lower the recorder pen and trigger a single sweep, and raise the pen after the sweep is completed. A two-channel plot may be obtained by switching the DISPLAY switch to the second channel and triggering a second sweep.

3.6.5 USE OF OSCILLOSCOPE CAMERA. An oscilloscope camera may be clamped to the 5-1/2-in. bezel of the Model 8000 CRT and used in the normal manner to make permanent recording of single- or dual-channel presentations.

3.6.6 SELECTION OF DISPLAY VERTICAL SENSITIVITY. The proper setting of the VERTICAL SENSITIVITY control for each channel will depend upon the device being tested and the test readout method desired.

a. For greatest accuracy, digital readout from the VERTICAL POSITION counters can be used for all test measurements, as described in Paragraph 3.6.3. The maximum sensitivity of 0.5 DB/DIV. is useful for this mode, and the VERTICAL POSITION Controls are used to return any desired measurement point(s) to the graticule centerline. The gain or loss measurements can then be read directly in db, in 0.1-db increments, from the digital counters.

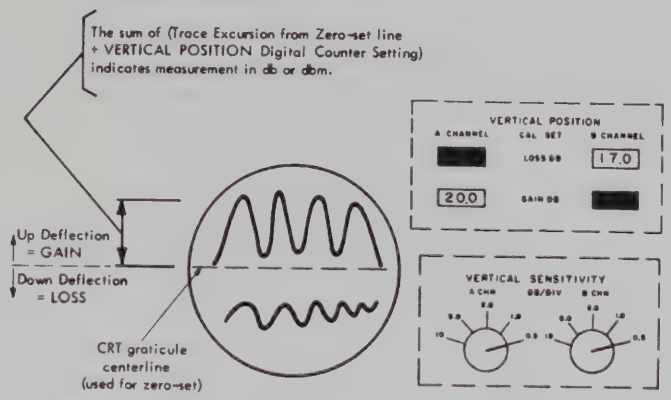
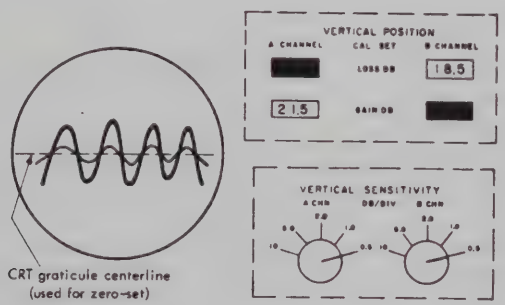
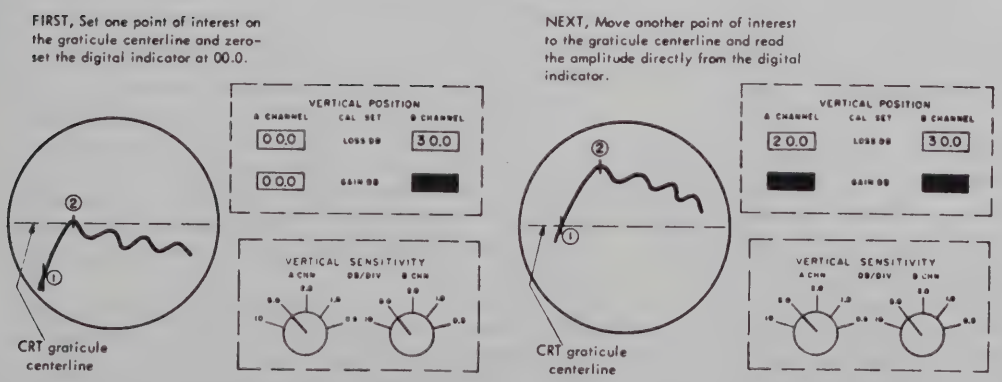


FIGURE 3-5. TYPICAL HIGH SENSITIVITY "QUICK-LOOK" PRESENTATION WHERE DIGITAL VERTICAL POSITION OFFSET IS USED TO BRING TRACE WITHIN CALIBRATED GRATICULE RANGE.



A. TYPICAL DUAL-CHANNEL HIGH SENSITIVITY READOUT WHERE THE DIGITAL VERTICAL POSITION INDICATOR IS USED TO OFFSET THE TRACE TO THE ZERO-SET LINE AT EACH DESIRED POINT OF MEASUREMENT.



B. TYPICAL HIGH SENSITIVITY READOUT WHERE TRACE AMPLITUDE BETWEEN POINTS (1) AND (2) IS EVALUATED BY USING THE DIGITAL VERTICAL POSITION INDICATOR. (SINGLE-CHANNEL CHN A APPLICATION ILLUSTRATED.)

FIGURE 3-6. TYPICAL HIGH RESOLUTION DIGITAL COUNTER READOUT

b. For quick-look evaluation of performance directly from the CRT, and for making a permanent record of the display by means of an X-Y recorder or oscilloscope camera, a VERTICAL SENSITIVITY setting that places the excursions of each trace within a convenient band on the graticule can be used. For such presentation of return loss, a setting of 2.0 or 5.0 DB/DIV. will often be useful. For presentation of transmission gain or loss, the setting to be used depends on the flatness of the performance characteristic of the device under test. To display the output of a leveled sweeper, the 0.5 DB/DIV. setting may be used. For testing an unleveled source or a passive component, a setting of 2.0 or 5.0 DB/DIV. will often be useful; in some cases, the 10 DB/DIV. sensitivity will be required to keep the trace within the desired viewing range.

NOTE: The use of the ratiometric measurement procedure obviates the need for a leveled rf source in the measurement system. It provides "flat" readout over the band where response of the device under test is flat, regardless of whether or not the rf source driving the test loop is leveled. This permits establishment of horizontal go/no go acceptance bands on either side of each zero-set line on the graticule, for instant evaluation of broadband swept performance, and permits use of high sensitivity settings to monitor flat performance. Note also that the advanced design of the 8000/7051 eliminates the need for 1 KHz amplitude modulation of the sweeper output, as was typical in older ratiometer systems.

3.7 PROCEDURE FOR INPUT BALANCING AND SELECTION OF ALTERNATE DISPLAY SWEEP METHODS.

3.7.1 GENERAL. When used with swept signal sources, the 8000/7051 can utilize a linear low-voltage sweep ramp signal supplied by the signal source to the INPUT HORIZONTAL jack to sweep the CRT presentation for a standard performance-vs-frequency readout display. If the sweep speed is faster than 1 second, and the swept signal source is an ALFRED Model 630, 640 or 650 Series, or equivalent, which turns the rf output completely off during retrace, automatic balancing may be used. With slower swept signals, when driving a recorder, or with swept signals which are not turned completely off during retrace, manual balancing is required periodically. When used with single-frequency signal sources, the 8000/7051 supplies its own line-frequency internal sweep signal to "spread" the display, and manual balancing is required periodically.

NOTE: To determine whether any response distortion is present in swept measurement displays, particularly at low power levels, reduce the sweep speed slightly and note whether any change takes place in the response shape. If response shape is independent of sweep speed, the sweep speed is not excessive. If response distortion is present, use a slower sweep.

3.7.2 DISPLAYING FAST SWEPT SIGNALS WITH AUTOMATIC BALANCING. With swept signals having a sweep time of 1 second or less, and if the rf output is turned completely off during each sweep retrace, proceed as follows:

a. Connect the oscillator dc sweep ramp output signal to the Model 7051 INPUT HORIZONTAL jack. The voltage should be a positive-going ramp with a maximum level ranging from 10 to 50 volts.

b. Make the following switch settings pertaining to display control (other switch settings depend upon operating mode as described in other paragraphs):

BALANCE Control switch to AUTOMATIC
HORIZONTAL POSITION Control to set the left-hand limit of the swept trace at the CRT graticule edge 5 cm left of center.
HORIZONTAL POSITION SENSITIVITY Control to set the right-hand limit of the swept trace at the right-hand graticule edge, 5 cm right of center.

NOTE: If a display obtained with automatic balance is to be X-Y recorded by slowing the sweep to more than 1 second, the manual balance mode should be used for the recording interval in accordance with Paragraph 3.7.3 below. In some cases a satisfactory check of balance can be made before changing to slow sweep, and without altering the measurement set-up to carry out the balance procedures of Paragraph 3.7.3. This check is permissible in all LOG mode measurements and in those RATIO mode measurements, such as in reflectometry, in which the power level applied to the REF channel is > 15 db greater than that applied to the A or B Channel being recorded. This simple check is made as follows: Turn the BALANCE switch back and forth between AUTO and MAN, and adjust the BALANCE control for the channel being monitored until there is no noticeable movement in the trace position. The instrument is then ready for slow-sweep operation in the MAN balance mode.

3.7.3 DISPLAYING FAST SWEPT SIGNALS WITH MANUAL BALANCING. If the rf output from the swept signal source is not turned completely off during retrace (e.g. some sweepers operate with power on during retrace and others reduce power a fixed amount, such as 30 db), the automatic balancing mode cannot be used regardless of sweep speed. In this case, proceed as follows:

a. Connect the oscillator dc sweep ramp output signal to the Model 7051 INPUT HORIZONTAL jack. The voltage should be a positive-going ramp with a maximum level ranging from 10 to 50 volts.

b. Make the following switch settings pertaining to display control (other switch settings depend upon operating mode as described in other paragraphs):

BALANCE Control switch to MANUAL
HORIZONTAL POSITION Control to a position that centers the swept presentation on the CRT graticule.
HORIZONTAL POSITION SENSITIVITY Control to a position that gives the desired sweep width.
VERTICAL SENSITIVITY to 0.5 DB/DIV.

c. Turn the rf output of the oscillator fully off, or temporarily disconnect the oscillator from the test loop, whichever is easier.

NOTE: Since the Model 7051 INPUT jacks are isolated, the crystal detector shell is normally grounded through its rf input connection. If the rf input connection is broken, provisions must be made to ground the detector shell to the Model 8000/7051 chassis. It is preferable to perform balancing with the same connection configuration that will be used for measurements, i.e. with rf power turned off, so that prevailing ground loops will be balanced out.

d. Turn the DISPLAY Mode Selector switch to A CHN BAL. If the trace is not exactly coincident with the graticule centerline, adjust the A CHN BALANCE screwdriver control to move the trace to graticule center.

NOTE: If you encounter difficulty in balancing when the rf source being used is a sweeper with PIN diode leveling, check for dc currents in the rf input line to the crystal detector due to leakage within the PIN diode modulator. Add a dc block in the rf source output line, if necessary, to eliminate this problem.

e. Turn the DISPLAY Mode Selector switch to REF CHN BAL. If the trace is not exactly coincident with the graticule centerline, adjust the REF CHN BALANCE screwdriver control to move the trace to graticule center.

f. Turn the DISPLAY Mode Selector switch to B CHN BAL. If the trace is not exactly coincident with the graticule centerline, adjust the B CHN BALANCE screwdriver control to move the trace to graticule center.

g. Turn the DISPLAY Mode Selector switch to the desired RATIO or LOG measurement position, restore the oscillator output power to the test loop, and carry out the desired measurements.

h. Every half hour, repeat steps c through f above, and again resume the measurement procedure. After several hours' operation rebalancing intervals may be made less frequent when the half-hour checks show no drift has taken place.

3.7.4 DISPLAYING SLOW SWEPT SIGNALS WITH MANUAL BALANCING. Swept signals having sweep speeds slower than 1 second must be used with manual balancing. If the sweep signal source supplies a suitable horizontal deflection signal, use the procedure given in Paragraph 3.7.3 above. If the sweep signal source does not supply a suitable horizontal deflection signal, the Model 8000/7051 internal sweep must be utilized. Use the procedure of paragraph 3.7.5 below.

3.7.5 DISPLAYING SWEPT OR SINGLE-FREQUENCY SIGNALS REQUIRING USE OF INTERNAL SWEEP. If the swept signal source used does not supply a suitable horizontal deflection signal, or if measurements are being made using single-frequency signals, the Model 8000/7051 internal sweep must be utilized. The internal sweep is a line-frequency sine wave, which will sweep the screen horizontally many times during a single slow sweep of the rf signal. The CRT display, therefore, for each measurement channel will consist of a horizontal trace which will move between the measurement limits over the band being swept. To use internal sweep, turn the HORIZONTAL POSITION SENSITIVITY control fully CCW to the INTERNAL SWEEP position. Then follow the remainder of the procedure given in steps b through h of Paragraph 3.7.3 above.

3.8 BASIC PROCEDURE FOR MAKING ABSOLUTE MEASUREMENTS (See Figure 3-7).

3.8.1 GENERAL. For absolute power level measurements, the detectors connected to Channels A and B can be used individually or simultaneously with an appropriate LOG setting of the DISPLAY Mode Selector switch. The REF Channel is not used for absolute power level measurements, but connections may be retained in that channel as desired without interferring with the operation of the instrument. Assuming that detector compensation calibration has already been performed in accordance with Paragraph 3.5 for the detectors being used, the measurement of absolute power can be performed in a simple 1 - 2 sequence: (1) Perform power level readout calibration to set the Model 7051 digital counters and the Model 8000 CRT trace position for calibrated direct dbm readout; then (2) Apply test signals to the detector(s) and read the power level instantly. Once step (1) has been performed, any number of test signals can be applied to the detector(s) for measurement. The detailed procedure is given in the two paragraphs below.

3.8.2 POWER LEVEL READOUT CALIBRATION. Calibrate each channel being used for absolute power level measurements, as follows:

a. With the instrument turned on as directed in paragraph 3.4, make the following control settings:

DISPLAY MODE Selector to LOG A CHN
DISPLAY BALANCE Control switch to AUTO
VERTICAL SENSITIVITY (Both A CHN and B CHN) to 0.5 DB/DIV.

NOTE: If an external rf power source is being used as a calibration reference generator, turn the DISPLAY BALANCE Control switch to MANUAL and use the internal sweep and manual balancing procedure specified in paragraph 3.7.5. Leave the internal CALIBRATOR turned OFF.

b. Set the CALIBRATOR Control to +20 DBM.

NOTE: Be sure the detector being used will operate up to +20 dbm. If not, calibrate and operate at a lower power level. If the power levels to be measured are known to be closer to some other level, set the CALIBRATOR Control to that level instead.

c. Connect the rf input terminal of the Channel A crystal detector to the Model 7051 OUTPUT CALIBRATOR jack, using suitable rf connecting hardware.

d. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW out of the PRESET position, adjust the red knob to position the trace on the center horizontal line of the graticule.

e. Turn the black A CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to preset the digital counter readout to the same level as the CALIBRATOR Control setting. The digital counter setting should be 20.0 GAIN DB unless the CALIBRATOR was set to some level other than +20 DBM in step b; for example, if the CALIBRATOR was set to -30 DBM in step b, set the digital counter to read 30.0 LOSS DB; and if the CALIBRATOR was set to 0 DBM in step b, set the digital counter to read 00.0 DB. After the digital counter is properly set, turn the black knob fully CCW, out of the PRESET position.

f. If Channel B will also be used for measurement, change the DISPLAY MODE Selector setting to LOG B CHN.

g. Connect the rf input terminal of the Channel B crystal detector to the Model 7051 OUTPUT CALIBRATOR jack, using suitable rf connecting hardware.

h. Repeat steps d through f, substituting the B CHANNEL VERTICAL POSITION controls and digital counter.

i. The VERTICAL POSITION digital indicators for both channels are now calibrated to read the incident power level in dbm for any signal located on the horizontal graticule line. The VERTICAL POSITION controls can be used to return any portion of the measurement trace

to the calibration line on the graticule for measurement readout. Alternately, with a VERTICAL SENSITIVITY control setting that provides an on-scale presentation, the incident power level may be measured by evaluating the trace deflection from the calibration line.

3.8.3 POWER LEVEL MEASUREMENT PROCEDURE. Use the following procedure to make power level measurements after Channels A and B have been calibrated in accordance with paragraph 3.8.2:

a. Connect the Channel A (and Channel B, if desired) detector(s) to the desired power pickoff point(s) of the instrument or system under test using suitable rf connecting hardware.

NOTE: The 8000/7051 system calibration performed under paragraph 3.6.2 calibrates the instrument to read power directly in dbm at the detector input where the CALIBRATOR OUTPUT power was connected in that procedure. If the detector is subsequently connected to a sampler, or if a coupler, pad, etc., is now connected between the detector and the point at which power is to be measured, the readings must be interpreted accordingly. Any attenuation added between the detector and the measurement point must be added algebraically to the counter reading, or the counter may be preset to allow for this (e.g. if 10 db is to be added between the detector and the signal after calibration, then use +20 dbm for calibration but set the counters to 30 DB GAIN).

b. With the instrument turned on as directed in paragraph 3.4, make the following control settings:

DISPLAY Mode Selector to the desired LOG setting for single or dual-channel measurement.
VERTICAL SENSITIVITY to the desired position for each channel (depends on readout mode desired; see paragraph 3.6)

HORIZONTAL POSITION, BALANCE Control switch } set in accordance with the signal source and display sweep mode used; see Paragraph 3.7

c. Read the measurement(s) in dbm from the CRT graticule and/or the VERTICAL POSITION digital counters, by adjusting the red VERTICAL POSITION knob as desired to restore the trace onto or near the calibration line. (See Paragraph 3.6 for a discussion of alternate readout modes.) The measurement value of the trace at any point is equal to the dbm level shown on the VERTICAL POSITION digital counter for the corresponding channel, altered by the trace excursion, if any, from the graticule line at which the digital counter was calibrated in Paragraph 3.8.2. Excursions above the calibration line represent a power increase, and excursions below the calibration line represent a power decrease. The amount of such increase or decrease can be evaluated in terms of the selected VERTICAL SENSITIVITY setting, and added algebraically to the digital counter reading. Note that if the digital counters were calibrated in accordance with Paragraph 3.8.2, + dbm readings (i.e. decibels above 1 milliwatt) will be shown in the GAIN DB window of each counter, and - dbm readings (i.e. decibels below 1 milliwatt) will be shown in the LOSS DB window of each counter.

The dbm value of trace excursions from the calibration line can be added algebraically to either type of reading; several examples are tabulated below:

DIGITAL COUNTER READING	TRACE EXCURSION	MEASUREMENT READOUT (DBM)
15.2 GAIN DB	+.4 (above cal line)	+15.2 +0.4 =+15.6 dbm
15.2 GAIN DB	-.6 (below cal line)	+15.2 -0.6 = +14.6 dbm
15.2 GAIN DB	0 (on cal line)	+15.2 dbm
23.7 LOSS DB	+.4 (above cal line)	-23.7 +0.4 = -23.3 dbm
23.7 LOSS DB	-.6 (below cal line)	-23.7 -0.6 = -24.3 dbm
23.7 LOSS DB	0 (on cal line)	-23.7 dbm

d. Repeat the above steps as desired for additional measurements at other test points or on other equipment. No recalibration is necessary as long as the black VERTICAL POSITION knobs are left CCW, out of the PRESET position.

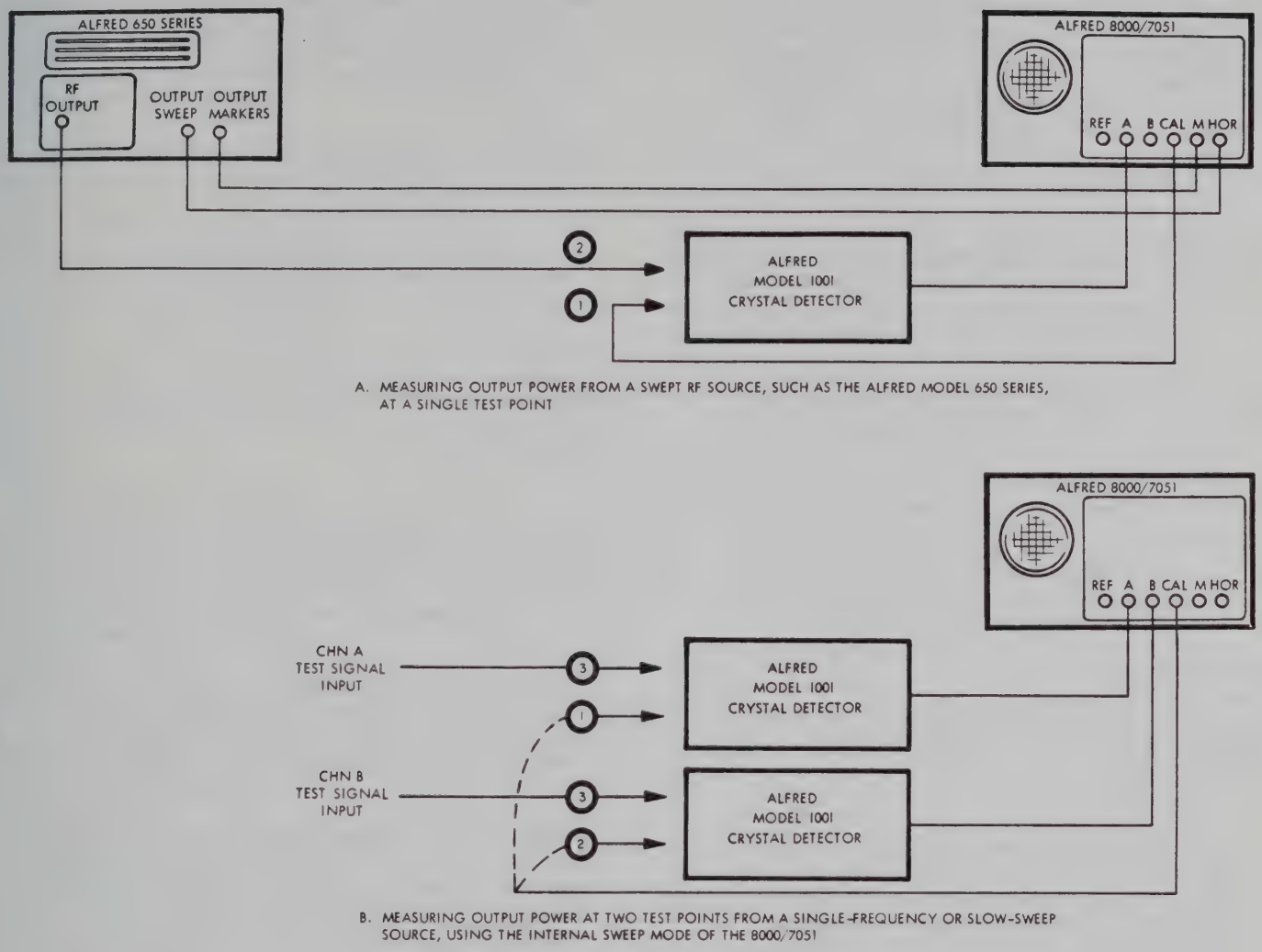
If a variety of tests are being made, involving tests at widely divergent power levels, it is recommended that the detector power level readout calibration be verified at the new level, using the procedure of Paragraph 3.8.2 for that level output from the internal calibrator.

3.9 BASIC PROCEDURE FOR MAKING GAIN/LOSS RATIO MEASUREMENTS (See Figure 3-8).

3.9.1 GENERAL. For power ratio measurements, the detectors connected to Channels A and B can be used individually or simultaneously, with an appropriate RATIO setting of the DISPLAY Mode Selector switch; and the REF Channel is used as the measurement reference for both channels. This instrument operates as two independent ratiometers with a common reference channel. The Channel A and Channel B readout indicates the ratio of the power incident on the detector for each channel to the power incident on the REF channel detector. Thus, the REF Channel is normally used to monitor drive power from the signal source, and the Channel A and Channel B detectors are used to measure response at two different points, such as reflected power at the input of the device under test (return loss or gain) and transmitted power through the device under test (transmission loss or gain).

In the set-up of Figure 3-8, conventional directional couplers and crystal detectors can be used to sample incident, reflected, and transmitted power to drive the REF, A, and B Channels of the 8000/7051. The ALFRED Crystal Detector Set, Model 1403 (consisting of three factory-checked Model 1001 Crystal Detectors), provides optimum broadband performance for signal levels up to +20 DBM.

It is desirable that the crystals and couplers shown in Figure 3-8 be matched. This permits response variations in the sampling elements to cancel. In cases where the transmitted power level is so low that the crystal must be connected directly to the output of the device under test, or where matched components are not available, the response variations in the sampling elements may be checked under test set-up conditions to obtain a correction factor for the display. A procedure for this is given in paragraph 3.13.3. For high power levels(> +20 dbm), suitable samplers or couplers can be used to reduce the incident power level applied to the detectors. Since the 8000/7051 does not require any rf source modulation, the rf source should be operated in an unmodulated mode.



A. MEASURING OUTPUT POWER FROM A SWEPT RF SOURCE, SUCH AS THE ALFRED MODEL 650 SERIES, AT A SINGLE TEST POINT

B. MEASURING OUTPUT POWER AT TWO TEST POINTS FROM A SINGLE-FREQUENCY OR SLOW-SWEEP SOURCE, USING THE INTERNAL SWEEP MODE OF THE 8000/7051

FIGURE 3-7. TYPICAL TEST CONNECTIONS FOR MEASUREMENT OF ABSOLUTE POWER LEVELS

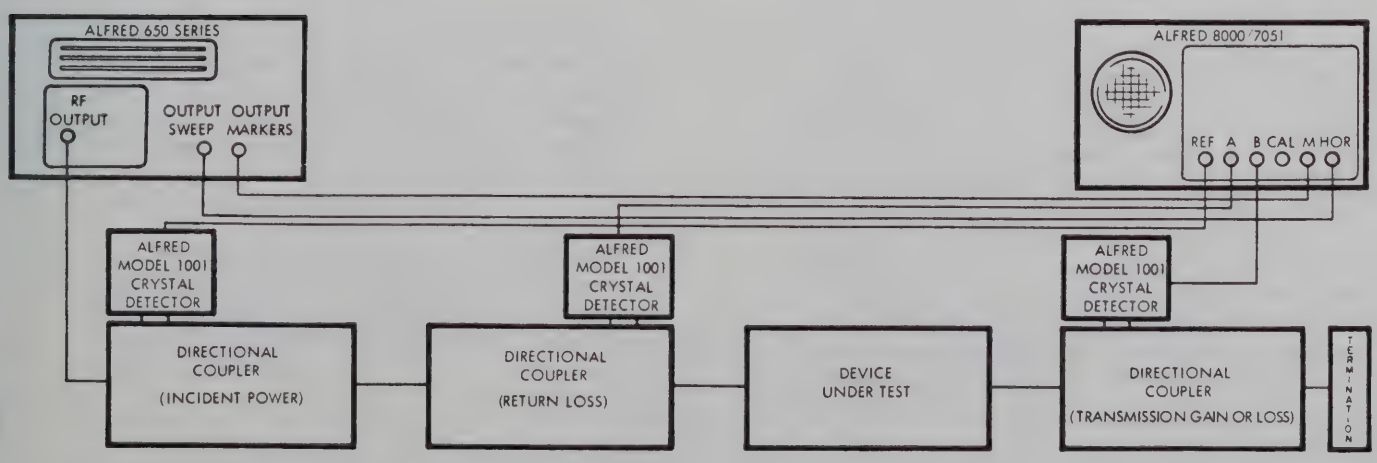


FIGURE 3-8. TYPICAL TEST CONNECTIONS FOR SIMULTANEOUS MEASUREMENT OF RETURN (VSWR) AND TRANSMISSION GAIN OR LOSS PERFORMANCE OF ACTIVE OR PASSIVE DEVICES

3.9.2 RATIO READOUT CALIBRATION. The basic test set up is shown in Figure 3-8. Once connections are arranged as shown to connect to the device under test, the set-up can be calibrated to compensate for sampler, coupler, and connection losses, by temporarily by-passing the device under test to "zero set" the Model 8000/7051 under no-gain, no-loss conditions. Proceed as follows:

a. With the instrument turned on as directed in Paragraph 3.4, make the following control settings:

DISPLAY Mode Selector to the desired RATIO setting for single or dual-channel measurement.
VERTICAL SENSITIVITY to the desired position for each channel (depends on readout mode desired; see Paragraph 3.6)

HORIZONTAL POSITION Controls, BALANCE Control switch } set in accordance with the signal source and display sweep mode used; see Paragraph 3.7

b. With connections designated as shown in Figure 3-8, disconnect the device under test from the primary output terminal of the reflected power sampler, and short this terminal with an ideal short. All incident power is now reflected. This condition represents 100% reflection or 0 db return loss.

c. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, adjust the red knob to set the trace corresponding to the 100% power reflection on the center horizontal line of the graticule.

d. Turn the black A CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to set the A CHANNEL digital counter to 00.0. After the digital counter is properly set turn the black knob fully CCW, out of the PRESET position. The Channel A Offset control counter is now calibrated to read return gain or loss directly in db; and the CRT presentation is also calibrated for direct db readout of trace excursions about the zero-set baseline, with a scale factor established by the setting of the A CHN VERTICAL SENSITIVITY control.

e. Remove the short from the primary output terminal of the reflected power sampler. Then connect the transmitted power coupler (or detector) directly to the primary output terminal of the reflected power sampler. All incident power is now coupled to the transmitted power coupler, which represents the 100% transmission condition (0 db GAIN or LOSS).

f. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW out of the PRESET position turn the red knob to set the resulting trace corresponding to 100% transmission on the graticule centerline (or other desired baseline).

g. Repeat step d, substituting the B CHANNEL VERTICAL POSITION controls and digital counter. The B Channel is now calibrated to read transmission gain or loss directly in db, and the CRT presentation is also calibrated for direct db readout of trace excursions about the zero-set baseline. An independent scale factor can be established for each channel by use of the separate VERTICAL SENSITIVITY controls.

h. Restore test connections as shown in Figure 3-8.

3.9.3 RATIO MEASUREMENT PROCEDURE. Once the Model 8000/7051 has been zero-calibrated for ratio readout with a particular test set-up configuration, following the procedure of paragraph 3.9.2, any number of devices can be tested in rapid sequence, with direct CRT or digital readout, as follows:

a. Check that test connections have been made in accordance with the connection configuration used for zero-calibration (see Figure 3-8).

b. With the instrument turned on as directed in Paragraph 3.4, make the following control settings:

DISPLAY Mode Selector to the desired RATIO setting for single or dual-channel measurement.
VERTICAL SENSITIVITY to the desired position for each channel (depends on readout mode desired; see Paragraph 3.6)

HORIZONTAL POSITION Controls, BALANCE Control switch } set in accordance with the signal source and display sweep mode used; see Paragraph 3.7

c. Read the gain and loss measurement(s) directly in db from the CRT graticule and/or the VERTICAL POSITION digital counters, by adjusting the red vertical position knob as desired to restore the trace onto or near the zero-calibration line. (See Paragraph 3.6 for a discussion of alternate readout modes.) The measurement value of the trace at any point is equal to the db level shown on the VERTICAL POSITION digital counter for the corresponding channel, altered by the trace excursion, if any, from the graticule line at which the digital counter was calibrated in Paragraph 3.9.2. Excursions above the calibration line represent a ratio increase (gain), and excursions below the calibration line represent a ratio decrease (loss). The amount of such increase or decrease can be evaluated in terms of the selected VERTICAL SENSITIVITY setting, and added algebraically to the digital counter reading. Note that if the digital counters were calibrated in accordance with Paragraph 3.9.2, db gain readings will be shown in the GAIN DB window of each counter, and db loss readings will be shown in the LOSS DB window of each counter. The db value of trace excursions from the calibration line can be added algebraically to either type of reading; several examples are tabulated below:

DIGITAL COUNTER READING	TRACE EXCURSION (DB)	CALCULATION	MEASUREMENT (DB)
15.2 GAIN DB	+.4 (above cal line)	+15.2 +0.4 = +15.6 db gain	= 15.6 db gain
15.2 GAIN DB	-.6 (below cal line)	+15.2 -0.6 = +14.6 db gain	= 14.6 db gain
15.2 GAIN DB	0 (on cal line)	+15.2 db	= 15.2 db gain
23.7 LOSS DB	+.4 (above cal line)	-23.7 +0.4 = -23.3 db gain	= 23.3 db loss
23.7 LOSS DB	-.6 (below cal line)	-23.7 -0.6 = -24.3 db gain	= 24.3 db loss
23.7 LOSS DB	0 (on cal line)	-23.7 db	= 23.7 db loss

d. Repeat the above steps as desired for additional measurements at other test points or on other equipment. Additional devices can be tested without recalibration or readjustment of the Model 8000/7051, as long as the same test set-up configuration is retained and the black VERTICAL POSITION knobs are left CCW, out of the PRESET position, to retain the established zero calibration. Thus, test operations can be carried out as fast as connections can be made to each successive device.

3.9.4 CONVERSION OF RETURN LOSS MEASUREMENTS TO IMPEDANCE PARAMETERS. To convert return loss measurements in db to VSWR or reflection coefficient values, use standard nomograms available in microwave reference books, (such as the Microwave Engineers' Handbook) or the following:

(1) Reflection coefficient equations:

$$\text{Return loss (db)} = -20 \log_{10} \rho = -20 \log_{10} \left[\frac{\text{VSWR}-1}{\text{VSWR}+1}\right]$$

or

$$\text{Reflection coefficient, } \rho, = = \text{antilog}_{10} \left[\frac{-\text{Return loss (db)}}{20}\right]$$

(2) VSWR equation:

$$\text{VSWR} = \frac{1+\rho}{1-\rho} \quad \text{and} \quad \rho = \frac{\text{VSWR}-1}{\text{VSWR}+1}$$

3.10 BASIC PROCEDURE FOR EVALUATING BOTH GAIN/LOSS RATIOS AND ABSOLUTE POWER LEVELS FOR A DEVICE UNDER TEST.

3.10.1 GENERAL. In some applications it is desirable to measure both gain/loss performance and absolute input or output levels of a device under test. The flexible Model 8000/7051 permits this to be done by a dbm comparison method without requiring recalibration of the controls once they are set for absolute power readout.

3.10.2 PROCEDURE. Proceed as follows:

a. Use the procedure of Paragraph 3.8 to make the desired input and/or output absolute level measurements directly in dbm, with the incident power sampler or detector driving Channel A and the transmitted power sampler or detector driving Channel B.

b. Subtract the input level from the output level in dbm to obtain the transmission gain or loss ratio in db. If power is unleveled, level variations in the swept source will appear in each measurement trace, but will cancel out in the subtraction if matched components are used. The insertion loss of the incident power sampler or coupler should be subtracted from the indicated incident power level to obtain the true power incident on the device.

c. If measurement of return loss or gain is also required, the Channel B sampler or detector must be reconnected to monitor reflected power, while the A Channel sampler or detector continues to monitor incident power. The return loss ratio can be obtained by subtracting the incident power dbm indication from the reflected power dbm indication.

3.11 FREQUENCY DOMAIN REFLECTOMETRY (RETURN LOSS) MEASUREMENTS IN MICROWAVE SYSTEMS.

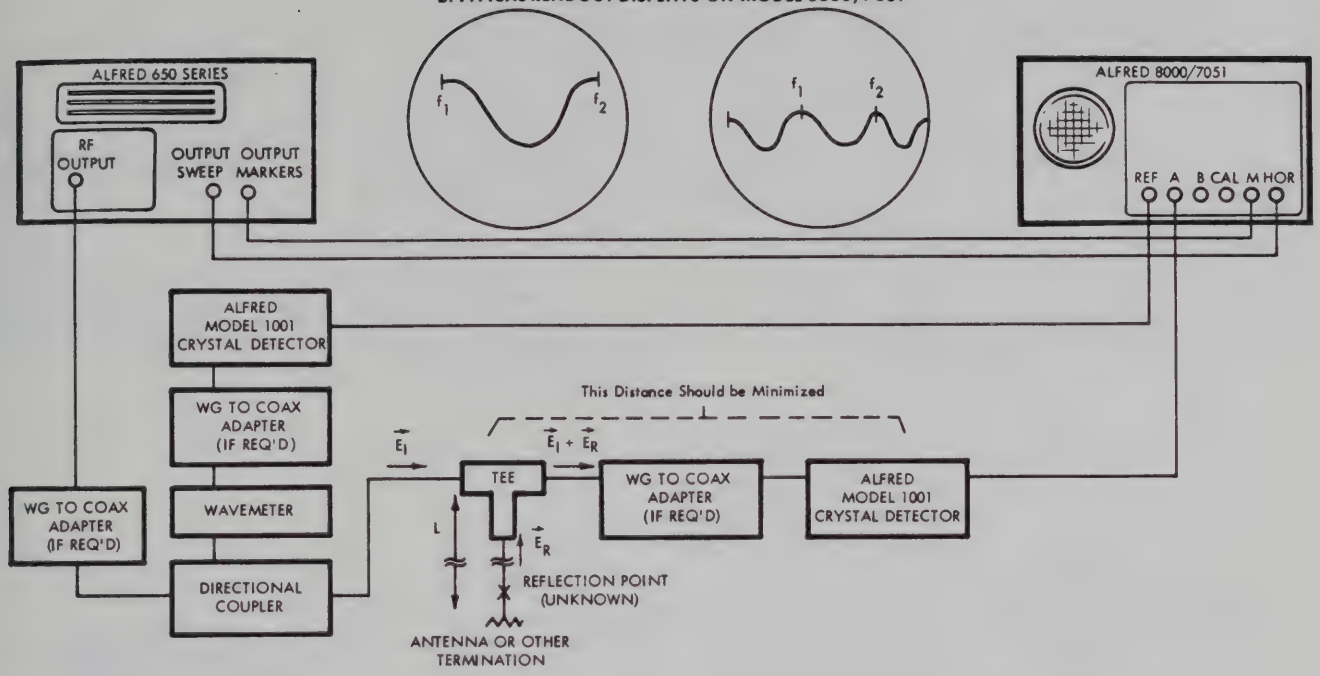
3.11.1 GENERAL. In applications involving microwave transmission and antenna systems, swept-frequency reflectometer measurements of return loss provide a simple and efficient technique for locating impedance discontinuities (faults). For a simple measurement of the total return loss of a component or system, the basic procedure of Paragraph 3.9 should be used for greatest measurement accuracy. To resolve the return loss of a complex system to estimate the amount and determine the location of each mismatch, a slightly different procedure is required. The procedure described here produces a "rippled" return loss display in which the ripple separation gives an indication of the distance to points of mismatch, and the ripple amplitude gives an indication of the magnitude of each mismatch.

A typical test set-up is shown in Figure 3-9 (A). The sweep signal generator output is connected to a tee coupler which drives the transmission system and the display detector. The transmission system need not be terminated. Any impedance discontinuities and/or termination mismatch will produce reflections which will combine with the incident signal in the tee coupler with a phase relationship that varies with both discontinuity distance (L) and signal frequency. The display will show "ripples" resulting from the vectorial addition of the signals at the Channel A crystal (Figure 3-9 (B) and (C)).

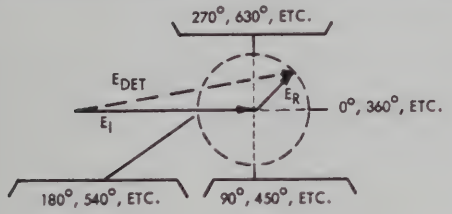
The frequency separation of the ripples is an indication of the distance of the discontinuity from the point of measurement, given by the equation for L in Figure 3-9 (C). A LOG A CHN display of the single detector output can be used to drive the display when incident power is leveled, because return loss can be determined from the display ripple variations without requiring a division by incident power. When the sweeper output is unleveled, a directional coupler should be used to sample the incident power level to drive the REF Channel crystal detector, with the instrument operated in the RATIO A ÷ REF mode. The

A. TYPICAL TEST SET-UP

B. TYPICAL READOUT DISPLAYS ON MODEL 8000/7051



C. DERIVATION OF FORMULA FOR DISCONTINUITY DISTANCE, L



E_{DET} = Vector Sum of $E_I + E_R$

Phase relationship of E_R to E_I, as illustrated above, is determined by the additional path length 2L traversed by the reflected signal, where L is the distance from the tee or hybrid coupler to the location of the discontinuity.

At frequencies such as f_1 and f_2 illustrated in B above, where L = an integral number of 1/2-wavelengths, the two signals reinforce to produce maximum detector output.

1. The ripple peaks are adjacent VSWR maxima which are displayed when the change in frequency makes the discontinuity distance change by 1/2 wavelength.
2. Thus, the change in wavelength between f_1 and f_2 times the total number of half-wavelengths at f_2 equals 1/2 wavelength at f_2.
3. Define: $\Delta\lambda = \left[\frac{cd}{f_1} - \frac{cd}{f_2}\right]$

   where c = free space velocity of light
   d = propagation constant which relates the propagation velocity in the waveguide or coax system to the velocity in free space
   $\Delta\lambda$ = change in wavelength between f_1 and f_2, $f_2 > f_1$

   $L' = \frac{ncd}{f_2}$

   where n = number of half-wavelengths to point of discontinuity
   L' = discontinuity distance
4. Restating (2)

   $ncd\left[\frac{1}{f_1} - \frac{1}{f_2}\right] = \frac{1}{2}\frac{cd}{f_2}$
5. Substituting from (3)

   $L' f_2\left[\frac{1}{f_1} - \frac{1}{f_2}\right] = \frac{1}{2}\frac{cd}{f_2}$
6. Simplify:

   $L'\left[\frac{f_2 - f_1}{f_1}\right] = \frac{1}{2}\frac{cd}{f_2}$
7. Solve for L:

   $L' = \frac{1}{2}\frac{cd}{(f_2 - f_1)} \cdot \frac{f_1}{f_2}$
8. Normalize to MHz with discontinuity distance measured in feet.

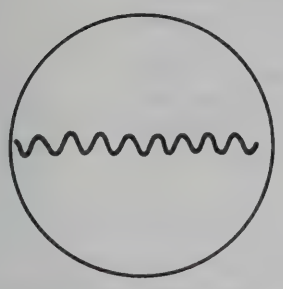
   $L = \frac{492\,d}{(f_2 - f_1)} \cdot \frac{f_1}{f_2}$

   where: f_2 and f_1 are the frequencies in MHz at which the maximum reflection occurs
   492 is the half-wavelength in feet of a 1-MHz wave in free space transmission
   d is the propagation constant, which relates the propagation velocity in the waveguide system to the velocity in free space
   L is the distance, in feet, from the tee or hybrid coupler to the discontinuity
9. Note that if f_1 and f_2 are close together, as with a narrow-band Δf sweep, which is required for discontinuity distances of any reasonable length at microwave frequencies,

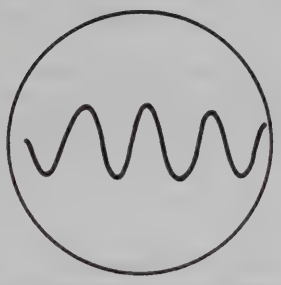
   the formula simplifies to

   $L \approx \frac{492\,d}{f_2 - f_1}$

FIGURE 3-9. FREQUENCY DOMAIN REFLECTOMETRY



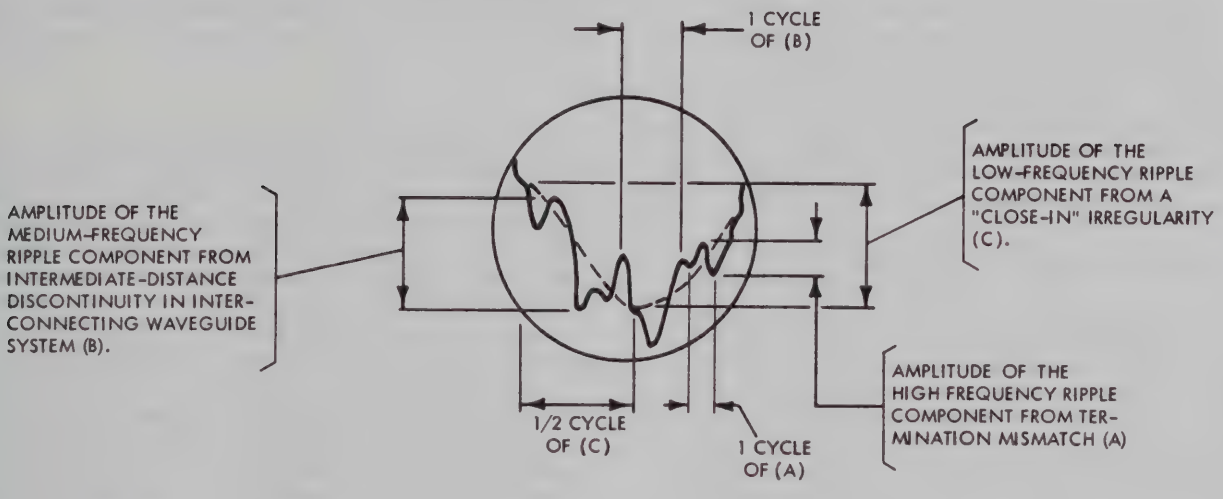
(A) Ripples from Termination only (Antenna, Feedhorn, etc.)



(B) Ripples from intermediate-Distance Discontinuity in interconnecting Waveguide System only

(C) Ripple from "Close In" Waveguide Defect

(D) Complex Wave addition of (A), (B) and (C)


1 CYCLE OF (B)
AMPLITUDE OF THE MEDIUM-FREQUENCY RIPPLE COMPONENT FROM INTERMEDIATE-DISTANCE DISCONTINUITY IN INTER-CONNECTING WAVEGUIDE SYSTEM (B).
AMPLITUDE OF THE LOW-FREQUENCY RIPPLE COMPONENT FROM A "CLOSE-IN" IRREGULARITY (C).
AMPLITUDE OF THE HIGH FREQUENCY RIPPLE COMPONENT FROM TER-MINATION MISMATCH (A)
1/2 CYCLE OF (C)
1 CYCLE OF (A)

(E) Visual Analysis of Complex Wave Shown in (D)

FIGURE 3-10. ANALYSIS OF COMPLEX REFLECTOMETRY DISPLAY

display then becomes independent of swept level variations which might otherwise introduce serious errors. Where a single discontinuity (or a termination of unknown match) is present, the distance, L, to the discontinuity or mismatch can be determined from the equation in Figure 3-9 (C), obtaining the applicable propagation constant (d) ($\approx \lambda/\lambda_g$) from a reference book such as the Microwave Engineers' Handbook. For greatest resolution in determination of L, use the $F_0 \pm \Delta F$ sweep with ΔF set to the lowest point that provides a double-maximum display, such as the left-hand oscillograph in Figure 3-9 (B). Then use the wavemeter to identify f_1 and f_2 accurately.

The approximate magnitude of the reflection (and therefore the impedance mismatch), can be determined easily from the direct db readout, by interpreting the display as a logarithmic standing-wave ratio presentation. The SWR in db, which is the peak-to-peak ripple amplitude, can be converted to a numerical VSWR using the Voltage Ratio scale on the Alfred Nomograph Slide Rule or the formula:

$$\text{VSWR} = \text{antilog}_{10} \frac{\text{SWR (db)}}{20}$$

Once the VSWR is known, the return loss can be determined from the Alfred Nomograph or from the formula

$$\text{Return Loss} = -20 \log_{10} \frac{\text{VSWR} - 1}{\text{VSWR} + 1}$$

In practical cases where multiple discontinuities (or one or more discontinuities plus an imperfect termination) are present, the display must be broken into its component parts by visual analysis in order to obtain the proper db and frequency values to use in the above equations for return loss and discontinuity distance. The reflections due to the multiple discontinuities will add to produce a complex display. Such a display can be broken into its component parts by analyzing it in terms of the following rules, as illustrated in Figure 3-10. Note that analysis becomes more difficult as the number of multiple discontinuities increases.

a. Complex wave is the sum of the individual return loss indications.

b. "Ripple frequency" increases with source distance in accordance with the equation given in Figure 3-9(C). Therefore the termination mismatch produces the most ripples, and a close-in defect may produce only an incomplete cycle.

c. Ripple amplitude of each component of the complex wave is related to its mismatch magnitude. Approximate Return loss can be determined from ripple amplitude by means of equation (3) above.

NOTE: For applications where multiple discontinuities need not be evaluated, the technique using directional couplers (Fig. 3-8 and Paragraph 3.9) provides a more accurate measurement of the net return loss.

3.11.2 PROCEDURE. Follow the general procedure for making return loss measurements given in Paragraph 3.9, but use the test set-up shown in Figure 3-9 and operate the sweep generator output in the narrow-band sweep mode to provide optimum ripple resolution on the CRT display. Interpret the display in accordance with the above discussion. When incident power is leveled and it is desired to omit the rf circuit to drive the REF Channel, the wavemeter may be inserted in the main rf circuit.

3.11.3 CALIBRATION OF CRT TO READ DIRECTLY IN DISCONTINUITY DISTANCE FOR COAX SYSTEMS. In coax systems it is possible to calibrate the CRT display to read directly in "feet per ripple" for applications where repetitive reflectometry measurements are to be made to locate points of damage or discontinuity in cables, etc. This is because coax is broadband and not frequency sensitive. The formula given in Fig. 3-9 above can be made to give an exact correlation of ripples to discontinuity distance in feet by selecting the numerator and denominator to be equal or related by an integer. Because of the shape of the sinusoidal ripples, it is easier to read the display accurately if there are five to ten ripples across the graticule. The calibration must therefore be established in accordance with the length of cable to be tested and/or the expected discontinuity distance to obtain multiple ripples.

Calibration may be established either (1) by cutting a sample cable to a nominal length and adjusting the sweep width to yield an integral number of ripples, or (2) by calculating the required sweep width using the propagation constant for the particular cable and setting the frequency limits with a wavemeter. When using the calculation technique, note that the propagation constant for many coaxial cables is either .659 or .695, so that a mean value of .677 may be used for general calibration, or the proper constant for the particular type of cable being used may be obtained from the manufacturer. Having determined the propagation constant, select values for f_2 and f_1 that make L an integral number of feet per ripple, or, for shorter cables, ripples per foot. Wherever possible, use a narrow-band $F_0 \pm \Delta F$ sweep mode. An example is given below:

Situation: S-band; probable length to fault ≈ 10 to 25 feet; d = .695.

Selection: Calibrate display to read 2 feet per ripple; therefore $f_2 - f_1$ must be selected to be half of (492 d) = 170.7 MHz.

Calibration: Either select two frequencies 170.7 MHz apart for the $F_1 \rightarrow F_2$ sweep limits, or set the total $F_0 \pm \Delta F$ excursion to be 170.7 MHz, using the wavemeter.

Alternate Calibration: Assemble a 15-foot length of cable of the type to be tested, having a connector on one end and the other end cut at exactly 15 feet. Adjust the $F_1 \rightarrow F_2$ sweep spread or the ΔF sweep width until exactly 7-1/2 full ripple cycles are displayed across the 10 scale-division width of the CRT between the graticule limit lines.

Measurement: Connect an unknown cable, and evaluate the number of ripples across the full 10 scale-division width of the CRT. The distance to the discontinuity point is 2 x the number of ripple cycles. If the display shows 10-3/4 ripples between the graticule limit lines, the discontinuity is 21-1/2 feet from the connector attached to the measurement set-up. In actual measurements the waveforms may be complex due to multiple reflections, but analysis of the display, plus some practice, should enable the operator to determine the discontinuity distance accurately.

NOTE: If calibration is once performed using method (2) with a wavemeter, this calibration may be preserved by preparing a snipped-off "calibration" cable cut to a length which gives a particular integral number of ripples on the display. To re-establish the measurement set-up at a different time or location, merely adjust the rf source sweep width to give the same number of ripples when this "calibration" cable is connected as the unknown.

3.12 BASIC PROCEDURE FOR NOISE FIGURE MEASUREMENTS (See Figure 3-11).

3.12.1 GENERAL. With the Model 8000/7051 System, swept noise figure measurements can be made using any noise source and without requiring auxiliary noise figure meters. The noise figure of a microwave receiver is a convenient specification of the overall effect of the various sources of noise in the receiver, and is defined as the ratio of the available signal-to-noise ratio at the input to the available signal-to-noise ratio at the output:

$$F = \frac{Si/Ni}{So/No}$$

The derivation of basic noise-figure formulas can be found in any standard reference. The noise figure in db can be expressed as:

$$F_{db} = 10 \log \frac{(T_2 - T_0)}{T_0} - 10 \log \left(\frac{N_2}{N_0} - 1\right) \qquad (4)$$

where the ratio $\frac{T_2 - T_0}{T_0}$ is an indication of the relative excess noise power available from the noise source, and is usually given in db by the noise source manufacturer

N_0 = noise detected at receiver output with noise source turned off and device input terminated

N_2 = noise detected at receiver output with noise source turned on

Where excess noise available from the noise source is specified by the manufacturer in db, the above equation simplifies to:

$$F_{db} = (\text{Excess Noise})_{db} - 10 \log \left(\frac{N_2}{N_0} - 1\right) \qquad (5)$$

The noise figure of an equipment under test, as defined by the above equations, can be measured simply and quickly on a swept basis, using the 8000/7051 system as a direct-reading power meter. A mixer is used to shift the noise output to the frequency of a narrow-band I.F. strip, and the noise monitored will thus be the average of the signal-and image-frequency noise. This will not produce measurement error unless the noise figure is significantly different at the two frequencies.

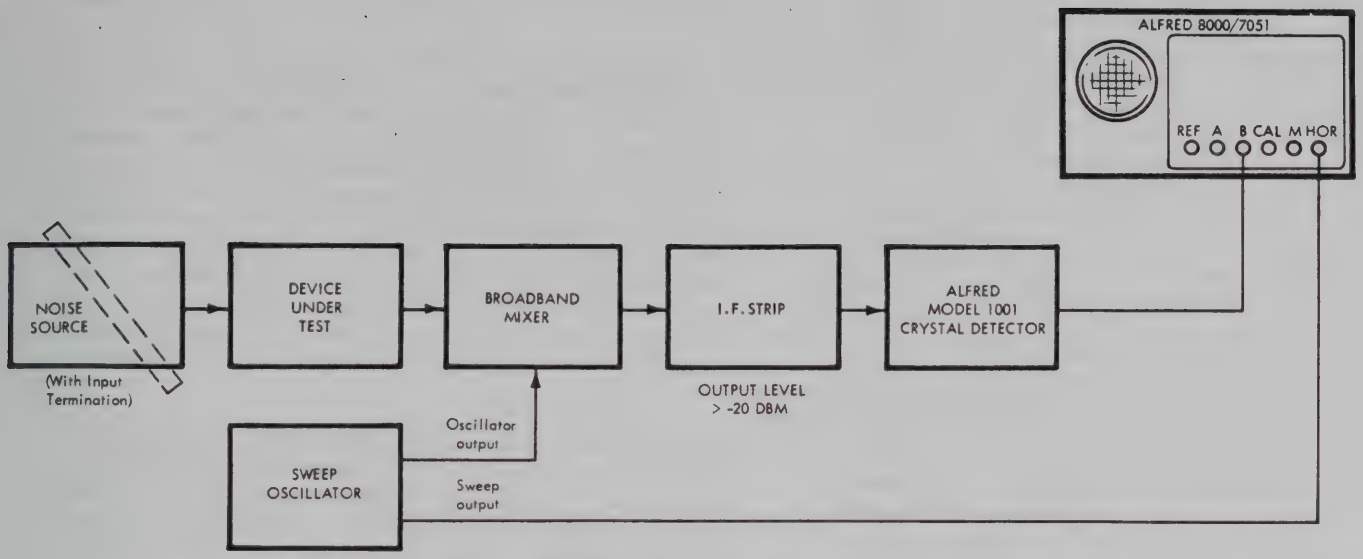


FIGURE 3-11. TYPICAL TEST CONNECTIONS FOR NOISE FIGURE MEASUREMENTS

3.12.2 PROCEDURE. Proceed as follows:

a. Make the test connections as shown in Figure 3-11. The noise source should provide a known excess noise figure over the frequency response range of the device under test. The sweep oscillator should be set to drive the broadband mixer over a frequency range separated from the desired test range by the operating frequency of the I.F. strip. Thus, the noise test signal amplified by the I.F. strip will sweep across the frequency range of the device under test.

b. With the Model 8000/7051 turned on as directed in Paragraph 3.4, make the following control settings:

DISPLAY MODE Selector to LOG B CHN
DISPLAY BALANCE Control Switch to MANUAL
(See Paragraph 3.7.3 for manual balancing procedure)
VERTICAL SENSITIVITY (B CHN) to 0.5 DB/DIV.

c. Turn on the device under test and all equipment in the test set-up except the noise source, to obtain a measurement of output level in the absence of excess noise.

d. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, adjust the red knob to position the trace on the center horizontal line of the graticule.

e. Turn the black B CHANNEL VERTICAL POSITION knob to the PRESET position. Then turn the red knob to preset the digital counter readout to read 00.0. After the digital counter is properly set, turn the black knob fully CCW, out of the PRESET position.

f. Turn the noise source on and use the red B CHANNEL VERTICAL POSITION knob to restore the trace to the center horizontal line of the graticule.

g. The GAIN DB indication for the B CHANNEL now indicates the ratio N_2/N_0 of the device under test in db (= 10 log N_2/N_0).

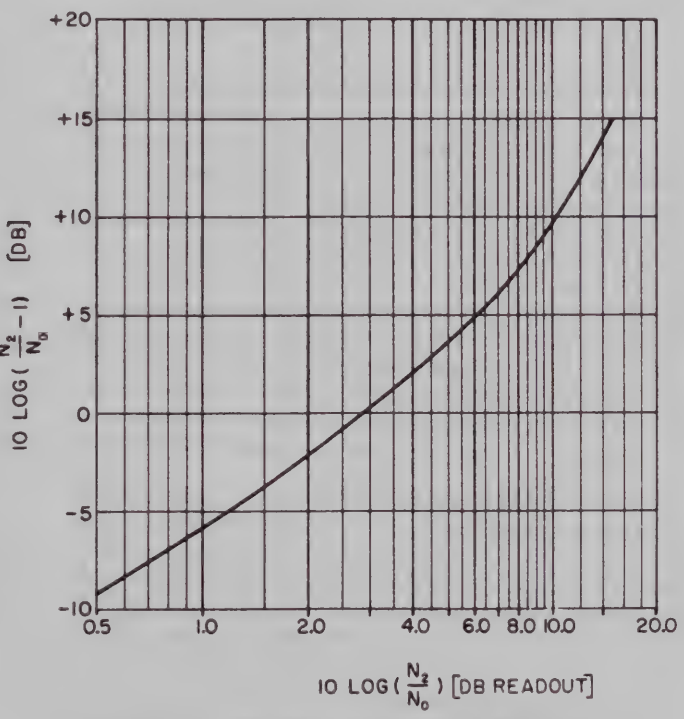


FIGURE 3-12. INTERPRETATION OF DB READOUT IN NOISE FIGURE MEASUREMENTS.

h. Convert the db reading of step g to a numeric ratio and solve equation (5) above to determine noise figure. (See graph in Figure 3-11 for conversion of the step g reading in db directly to the value 10 log ($N_2/N_0 - 1$) in db.

For example, if the excess noise from the sources is 15.2 db and the reading in step g is 5 db, N_2/N_0 = 3.16 and equation (5) reduces to

$$F_{db} = 15.2 \text{ db} - 3.35 \text{ db} = 11.85 \text{ db}.$$

If the reading in step g is 0.5 db, N_2/N_0 =1.122, and equation (5) reduces to

$$F_{db} = 15.2 \text{ db} - -9.15 \text{ db} = 15.2 \text{ db} + 9.15 \text{ db} = 24.35 \text{ db}$$

3.13 TYPICAL TEST & MEASUREMENT APPLICATIONS AND PROCEDURES.

3.13.1 COUPLER VSWR AND DIRECTIVITY MEASUREMENTS.

To measure the VSWR, coupling factor, and directivity of a coupler, make connections as shown in Figure 3-13. This data is obtained by making ratio measurements, using the basic procedures given in Par. 3.9. The transmitted power detector (or matched coupler) is connected to the secondary output arm of the coupler under test, to monitor power with the B Channel, thereby providing direct readout of coupling factor in db. The termination used on the coupler mainline output must have a very low VSWR or else a sliding termination should be used. The measurement of coupler parameters is illustrative of how the basic ratio measurement procedure can be easily adapted to nearly any measurement application.

Calibrate as directed in Par. 3.9, connecting the B Channel detector (or matched coupler) directly to the main output port of the reflected power coupler which drives the A Channel. The measurements then made with Channels A and B connected as shown in Figure 3-13 provide readout of return loss and coupling factor, respectively.

To measure directivity, leave the B Channel connected to the coupler arm and switch the rf input connection to the opposite port of the primary line so that the direction of mainline power flow is reversed in the coupler under test. Subtract the Coupling Factor DB LOSS ratio first measured on Channel B from the DB LOSS ratio now measured, to determine directivity in db.

> NOTE: If the detector is connected directly to the secondary output arm of the coupler in this procedure, the ratio measurements for coupling factor and directivity actually compare the response flatness of the incident power coupler (which drives the REF Channel) and the coupler under test; and the incident power coupler should be maximally flat for best results. The zero-set calibration trace will indicate the character of the non-flat response not due to the coupler under test, and this trace can be marked on the graticule with grease pencil, for subtraction from the subsequent performance trace. If a leveled source is available which has less db variation over the band than does the coupler available for incident power sampling, it is preferable to make a LOG B measurement for coupling factor and directivity using leveled power, instead of a RATIO measurement. In either case, the B Channel zero-set should be performed with the B Channel detector connected to the main output port of the reverse power coupler.

A maximally flat coupler usually has low directivity, which produces error in the reflected power (VSWR) measurement, (see Par. 3.14.1 for details). To avoid this error and substantially reduce the non-flat response not due to the coupler under test, it is advantageous to use high-directivity couplers, with a transmitted power coupler which is matched to the incident power coupler sampling the signal for the B Channel detector, in making ratio measurements for coupling factor and directivity. The frequency response variations of these matched couplers will then cancel, and the calibration trace will be practically horizontal, so that the measurement trace provides simple, direct readout of the non-flat response due to the coupler under test. In testing couplers having low directivity and/or large coupling factor, with sweeper output power of 20 mw or greater, the power levels available at the secondary output arm of the coupler under test during directivity measurements should be sufficiently above -40 dbm to permit use of a transmitted power coupler. When testing couplers having high directivity or small coupling factor it may be necessary to connect an amplifier to the sweeper output to supply sufficient power to permit use of a matched coupler at the secondary arm of the coupler under test. The ratio measurement technique permits a "flat" test loop independent of incident power variations.

3.13.2 SIMULTANEOUS MEASUREMENT OF FILTER VSWR AND INSERTION LOSS.

To measure the VSWR and insertion loss of a filter, make connections as shown in Figure 3-8. These measurements are again performed with the ratio technique, using the basic procedures given in Par. 3.9. Measure reflected power with a reverse sampler driving the A Channel, and measure transmitted power with a sampler connected to the filter output and driving Channel B. To extend the measurements over several octaves of frequency, merely switch RF plug-in units in the ALFRED Model 650 Sweep Oscillator and change the samplers or couplers as necessary. All other test connections remain the same. With the Model 8000/7051, there is no requirement for a group of costly precision variable attenuators to cover the frequency ranges under test.

NOTE: When measuring the VSWR of a device such as a filter which may have low insertion loss over a portion of the measurement frequency band, the transmitted power sampler and termination must present a low VSWR at the filter output, to avoid error due to power reflected from the device output mismatch. Alternately, the transmission sampler can be replaced by a precision termination during the VSWR measurement.

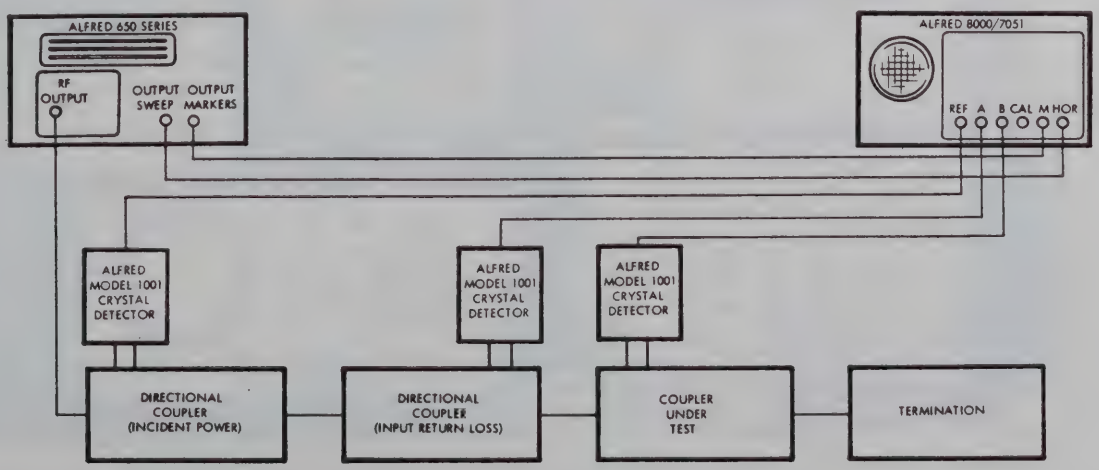


FIGURE 3-13. TYPICAL TEST CONNECTIONS FOR DIRECTIONAL COUPLER PERFORMANCE MEASUREMENTS.

3.13.3 SIMULTANEOUS MEASUREMENT OF AMPLIFIER VSWR AND INSERTION GAIN.

To measure input VSWR and transmission gain of a component simultaneously, make connections as shown in Figure 3-8. An equivalent test set-up showing test of an ALFRED 560 Series Microwave Amplifier is illustrated in Figure 3-14. To calibrate the A Channel RF test loop, short the primary output of the reflected power coupler, and set the resulting 0 db return loss indication to center scale (or other desired baseline) on the CRT. Then set the A Channel Offset control to 0 db after turning the concentric knob to disengage the counter drive from the potentiometer. To calibrate the B Channel RF test loop, the transmitted power coupler is connected directly to the reflected power coupler, and the display is similarly set to 0 db.

NOTE: Be sure to consider the power output of the amplifier when selecting the proper coupling factor for the transmitted power coupler. The crystal power rating is +20 dbm. A 10-watt amplifier usually has output power in excess of +40 dbm, so a 30 db coupler should be used.

For greatest accuracy, zero-set both channels to center scale. The Offset controls can then be used to restore the trace exactly to the scale centerline at any desired point or points in the horizontal sweep. This makes the gain or loss value at the desired point directly readable from the Offset control counter with no CRT interpolation required. This method is particularly useful for high sensitivity examination of performance. Gain measurements are indicated directly in db. Return loss measurements, also indicated directly in db, can be converted to VSWR values by reference to standard nomographs such as contained in the Microwave Engineers' Handbook or on the ALFRED NOMOGRAPH Slide Rule.

For "quick-look" wide band swept presentations that take full advantage of the readout speed of this new system, the two traces can be read from the CRT. With suitable zero-set and sensitivity settings, the performance tolerance for each parameter measured can be marked as an acceptance band on the CRT graticule to allow "at-a-glance" go/no-go evaluation. Note that the use of ratiometric measurements provides flat readout over the range where the response of the device is flat. A typical dual-channel readout is illustrated in Figure 3-15.

3.13.4 AMPLIFIER RF POWER OUTPUT MEASUREMENT.

To measure absolute power output of the amplifier tested above, switch the DISPLAY Mode Selector from RATIO to LOG presentation. Then disconnect the transmitted power detector and connect it to the CALIBRATOR output to drive the detector at a level close to that expected, such as +10 dbm, taking into account the db loss of the coupler or pad which will be used in the rf measurement to drop the level to within the crystal range (< +20 dbm). Zero-set the CRT display and then adjust the offset control counter to read a level equal to the calibrated level plus the db loss of the coupler or pad which will be used in the rf measurement. (See Par. 3.8 for the detailed Calibration Procedure.) Then connect the detector through a suitable coupler or pad to the output of the device under test and return the trace to the calibrated scale point using the VERTICAL POSITION Offset control. The Offset control now reads the absolute power directly.

"Quick-look" absolute power readout can also be utilized with proper sensitivity settings, to enable readout of the wideband response without readjustment of the Offset control. With a sensitivity setting of 5 db/cm, the full band unleveled power can be displayed for "quick-look" evaluation. For an internally leveled source, such as some models of the ALFRED 650 Series, a setting of 0.5 db/cm will permit similar evaluation of the leveled performance across the band.

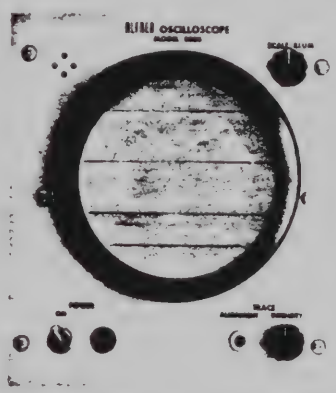


FIGURE 3-15. TYPICAL DUAL-CHANNEL CRT READOUT FOR AMPLIFIER TEST.

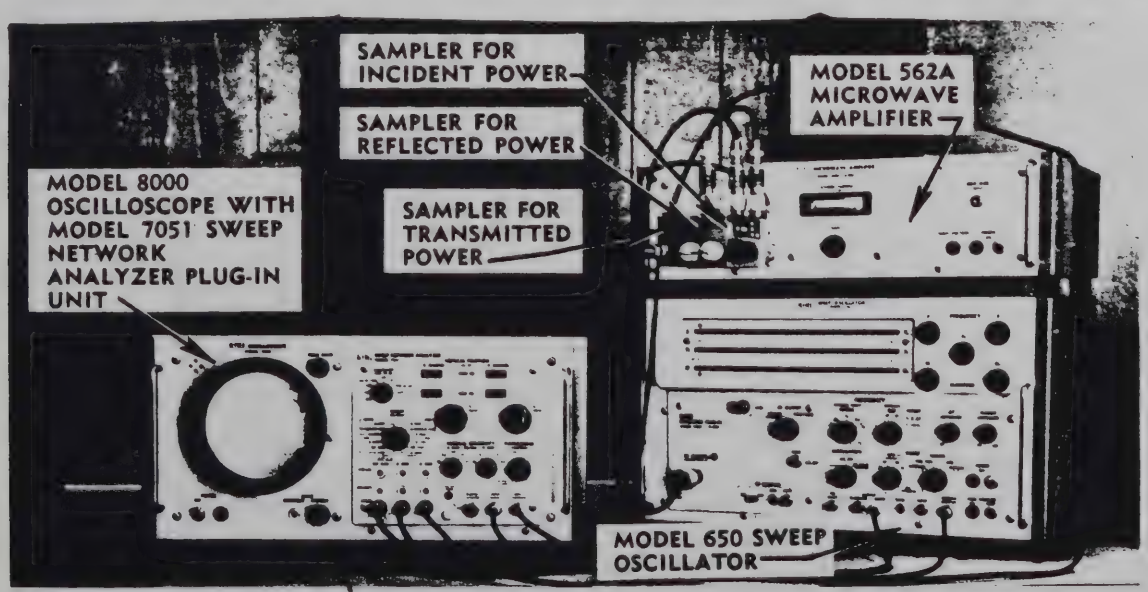

SAMPLER FOR INCIDENT POWER
SAMPLER FOR REFLECTED POWER
SAMPLER FOR TRANSMITTED POWER
MODEL 562A MICROWAVE AMPLIFIER
MODEL 8000 OSCILLOSCOPE WITH MODEL 7051 SWEEP NETWORK ANALYZER PLUG-IN UNIT
MODEL 650 SWEEP OSCILLATOR

FIGURE 3-14. TYPICAL TEST SET-UP FOR SIMULTANEOUS VSWR AND INSERTION GAIN MEASUREMENTS ON AN AMPLIFIER.

3.13.5 MEASUREMENT OF SIGNAL LEVELS AT DIFFERENT FREQUENCIES, FOR TESTING CONVERTERS, MIXERS, RECEIVERS, ETC.

Since the Model 8000/7051 measurement system is not frequency-restricted, it can be used to simultaneously measure the ratio or the absolute levels of signals at two frequencies. It can also measure the ratio of signal levels at two different frequencies to a reference signal at a third frequency. This capability permits simple one-step test and adjustment of converters, mixers, and receiver systems where signal levels at two or more different frequencies must be simultaneously evaluated.

A typical test set-up is shown in Figure 3-16. Directional couplers suitable for the frequencies involved are used to sample input and output power. If a simultaneous reflected power measurement is desired at the device input port, a reflected power sampling coupler can be inserted between the incident power coupler and the device under test to drive the remaining channel of the Model 8000/7051.

The ratio measurement procedure should be carried out as described in Par. 3.9, except that the output/input ratio zero-set calibration usually must be performed differently because the frequency-response limitations of the input and output couplers, which may operate in different bands, does not allow standard "zero set" calibration (at the input frequency) with the device under test removed from the circuit. However, if the output level is < +20 dbm (directly or through a suitable pad), and if no measurement of input reflected power is required, so that matched high directivity couplers (which reduce error in reflectometer measurements) need not be used, the test set-up shown in Fig. 3-16 may be modified by connecting the output detector directly to the device output, and using a maximally flat coupler to sample input power. Then, for zero-set calibration the output detector can be connected to the mainline output port of the incident power coupler; and the zero-set procedure can be carried out as described in Paragraph 3.9.2.

In cases where (1) An input VSWR measurement is to be made, requiring use of high directivity couplers which are not maximally flat but which can be obtained to "track" as closely as possible in db coupling variation over their respective bands; or (2) Where a maximally flat input coupler is not available or it is more convenient to use a coupler for output sampling, choose directional couplers that track as closely as possible in db coupling variation over their respective bands. The zero-set and measurement procedure given in Par. 3.9 applies directly to reflected power measurements at the device input. For output/input signal conversion ratio measurements, perform "zero-set" for different-frequency measurements by making a calibration adjustment to equalize inverse ratio readouts under actual measurement conditions, as follows:

a. Without making any "standard" zero-set adjustment, and with the black B CHANNEL VERTICAL POSITION knob fully CCW, out of the PRESET position, operate the instrument to make a RATIO B ÷ REF presentation. (The presentation can be swept or single-frequency.) Adjust the red VERTICAL POSITION knob to position the measurement trace on the horizontal graticule centerline, and note the reading in GAIN DB or LOSS DB on the B CHANNEL VERTICAL POSITION digital counter.

b. Interchange the rf input connections of the crystal detectors driving the REF and B Channels, (i.e., switch the B Channel detector to the input directional coupler, and switch the REF Channel detector to the output directional coupler. Adjust the red VERTICAL POSITION knob to return the trace to the horizontal graticule centerline. If the instrument happens to be properly "zero-set" for ratio measurements in this test set-up, the reading on the B CHANNEL VERTICAL POSITION digital counter will be the same numerically as in step a, but will appear in the alternate window. (e.g. A reading of 20.0 GAIN DB in step a and 20.0 LOSS DB in step b or vice versa indicates proper calibration.) If the readings are not identical numerically, determine the total ratio excursion which they represent. Do this by adding the two readings in db if one is a GAIN and the other a LOSS reading; alternately, if both readings are in the same window, subtract the smaller from the larger. Divide the resulting total db excursion by two to get the proper ratio reading for either test condition.

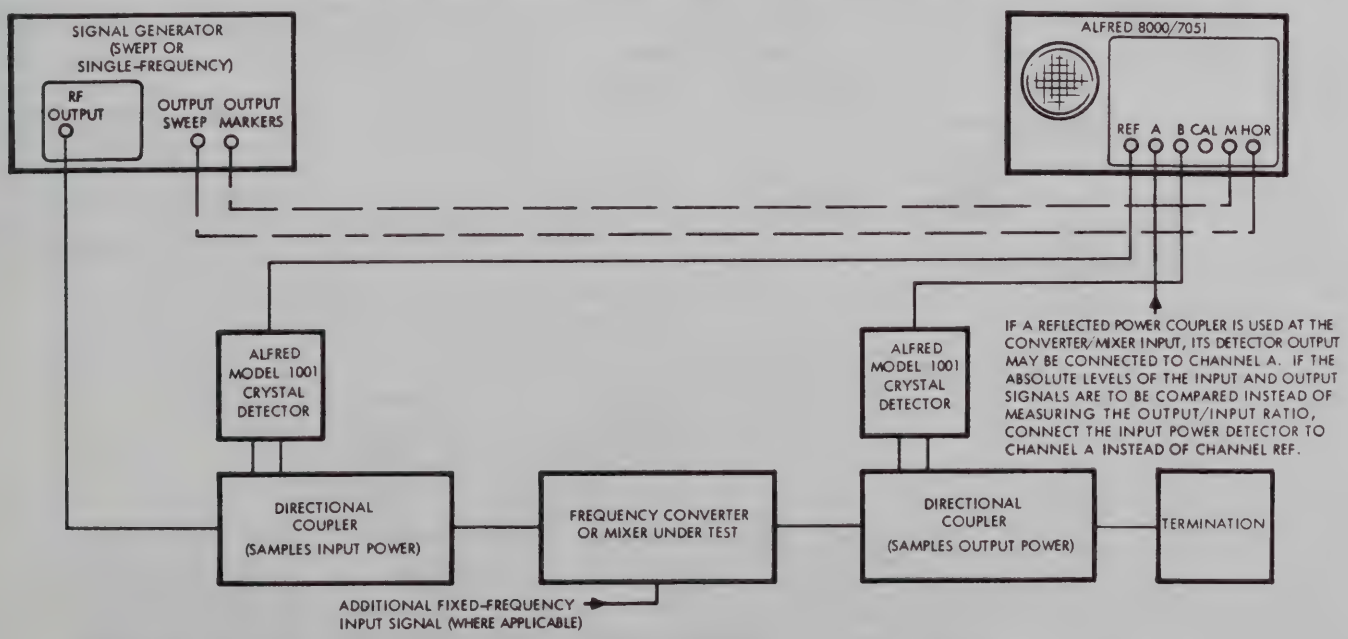

SIGNAL GENERATOR (SWEPT OR SINGLE-FREQUENCY)
RF OUTPUT
OUTPUT SWEEP
OUTPUT MARKERS
ALFRED 8000/7051
REF A B CAL M HOR
ALFRED MODEL 1001 CRYSTAL DETECTOR
ALFRED MODEL 1001 CRYSTAL DETECTOR
IF A REFLECTED POWER COUPLER IS USED AT THE CONVERTER/MIXER INPUT, ITS DETECTOR OUTPUT MAY BE CONNECTED TO CHANNEL A. IF THE ABSOLUTE LEVELS OF THE INPUT AND OUTPUT SIGNALS ARE TO BE COMPARED INSTEAD OF MEASURING THE OUTPUT/INPUT RATIO, CONNECT THE INPUT POWER DETECTOR TO CHANNEL A INSTEAD OF CHANNEL REF.
DIRECTIONAL COUPLER (SAMPLES INPUT POWER)
FREQUENCY CONVERTER OR MIXER UNDER TEST
DIRECTIONAL COUPLER (SAMPLES OUTPUT POWER)
TERMINATION
ADDITIONAL FIXED-FREQUENCY INPUT SIGNAL (WHERE APPLICABLE)

FIGURE 3-16. MEASUREMENT OF RELATIVE OR ABSOLUTE SIGNAL LEVELS AT DIFFERENT FREQUENCIES. (TYPICAL TEST OF FREQUENCY CONVERTER/MIXER IS ILLUSTRATED.)

Example A:

Reading in step a is 30.0 GAIN DB
Reading in step b is 10.0 LOSS DB
Total excursion = 30.0 + 10.0 = 40.0 DB

$$\text{Correct ratio} = \frac{40.0\ \text{DB}}{2} = 20.0\ \text{DB}$$

Reset the indicator in step b (by turning the black B CHANNEL VERTICAL POSITION knob CW to the PRESET position and then adjusting the red knob) to read 20.0 DB LOSS with the trace on the graticule centerline. Then restore the black knob to the fully CCW position (out of PRESET).

When connections are restored to the desired configuration of step a, the reading should be 20.0 DB GAIN.

Example B:

Reading in step a is 45.0 GAIN DB
Reading in step b is 16.2 GAIN DB
Total excursion = 45.0 - 16.2 = 28.8 DB

$$\text{Correct ratio} = \frac{28.8\ \text{DB}}{2} = 14.4\ \text{DB}$$

Reset the indicator in step b (by turning the black B CHANNEL VERTICAL POSITION knob CW to the PRESET position and then adjusting the red knob) to read 14.4 DB LOSS with the trace on the graticule centerline. Then restore the black knob to the fully CCW position (out of PRESET).

NOTE: The above calibration procedure, once understood, can be performed faster than it can be read. Once calibrated, the test set-up is ready for any number of measurements. Full-band calibration may be checked, if desired, by similarly evaluating other points.

c. Restore detector input connections as shown in Fig. 3-16. The instrument will now provide direct db readout of the output/input signal level ratio. Additional devices may be tested in the same set-up without requiring another zero-set adjustment.

NOTE: For output/input ratio measurements where signals in waveguide are involved and/or detectors cannot be interchanged for zero-set purposes, it is also possible to calibrate the instrument for absolute level measurements and determine the output/input ratio by subtracting one dbm reading from the other.

3.13.6 MEASUREMENT OF THE HARMONIC CONTENT OF A SIGNAL.

The broadband measurement capability of the Model 8000/7051 makes quick evaluation of harmonic content possible without requiring use of a separate spectrum analyzer instrument. A typical coaxial test set-up is shown in Figure 3-17. The directional coupler used should be maximally flat to minimize the frequency response error in the measurement. Suitable filters are used to separate the fundamental and desired harmonics, for measurement on separate channels of the Model 8000/7051. The main line of the coupler is used for the harmonic frequency measurement circuit to avoid high frequency coupling loss.

A low-pass filter with cut-off above the highest fundamental frequency in the sweep can be used to apply just the fundamental frequency level to the REF Channel. A high-pass filter with cut-off between the highest fundamental and the second harmonic of the lowest fundamental can be used to apply all harmonics to the A Channel.

The measurement procedure for coaxial systems can be performed in accordance with the general procedure for ratio measurements given in Par. 3.9. A single-channel ratio measurement is used, with a test set-up using a single directional coupler as illustrated in Figure 3-17. The "fundamental" signal detector drives the REF Channel, and the "harmonic" detector drives the A Channel. For zero-set calibration, remove the filters temporarily and set the RATIO A ÷ REF display to 00.0 with the trace on the horizontal centerline of the graticule. This calibration neglects filter insertion loss. If it is preferred to perform zero-set calibration with the filters in the circuit, the method of interchanging detector rf input connections for zero-set can be used, as in the technique given above for measurements of different-frequency signals. Once zero-set, the set-up can be used repetitively to test a variety of signals without further calibration.

NOTE: For systems in which harmonics of interest fall within waveguide bands (above 12.4 GHz), or if preferred for other frequency ranges, the harmonic signal content can be evaluated by comparing absolute signal level measurements, using suitable (waveguide) detectors. For an unleveled source and in coaxial systems, a ratio measurement is more convenient.

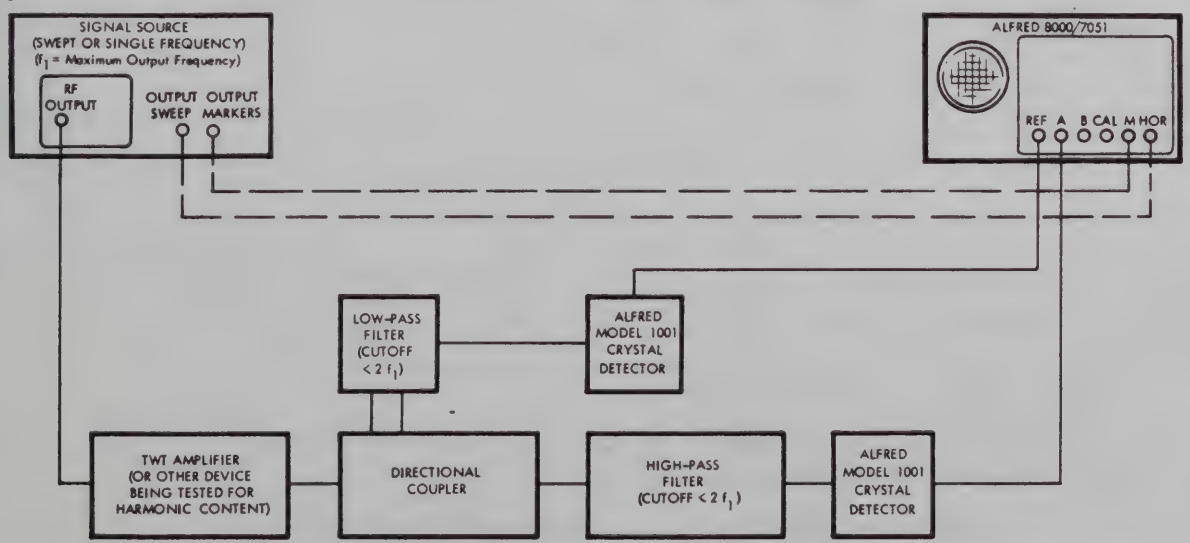

SIGNAL SOURCE
(SWEPT OR SINGLE FREQUENCY)
(f_1 = Maximum Output Frequency)
RF OUTPUT
OUTPUT SWEEP
OUTPUT MARKERS
ALFRED 8000/7051
REF A B CAL M HOR
LOW-PASS FILTER (CUTOFF < 2 f_1)
ALFRED MODEL 1001 CRYSTAL DETECTOR
TWT AMPLIFIER (OR OTHER DEVICE BEING TESTED FOR HARMONIC CONTENT)
DIRECTIONAL COUPLER
HIGH-PASS FILTER (CUTOFF < 2 f_1)
ALFRED MODEL 1001 CRYSTAL DETECTOR

FIGURE 3-17. MEASUREMENT OF HARMONIC CONTENT IN A SIGNAL BY SEPARATING THE FUNDAMENTAL FROM THE HARMONICS WITH FILTERS AND RATIOING THE SEPARATED SIGNALS.

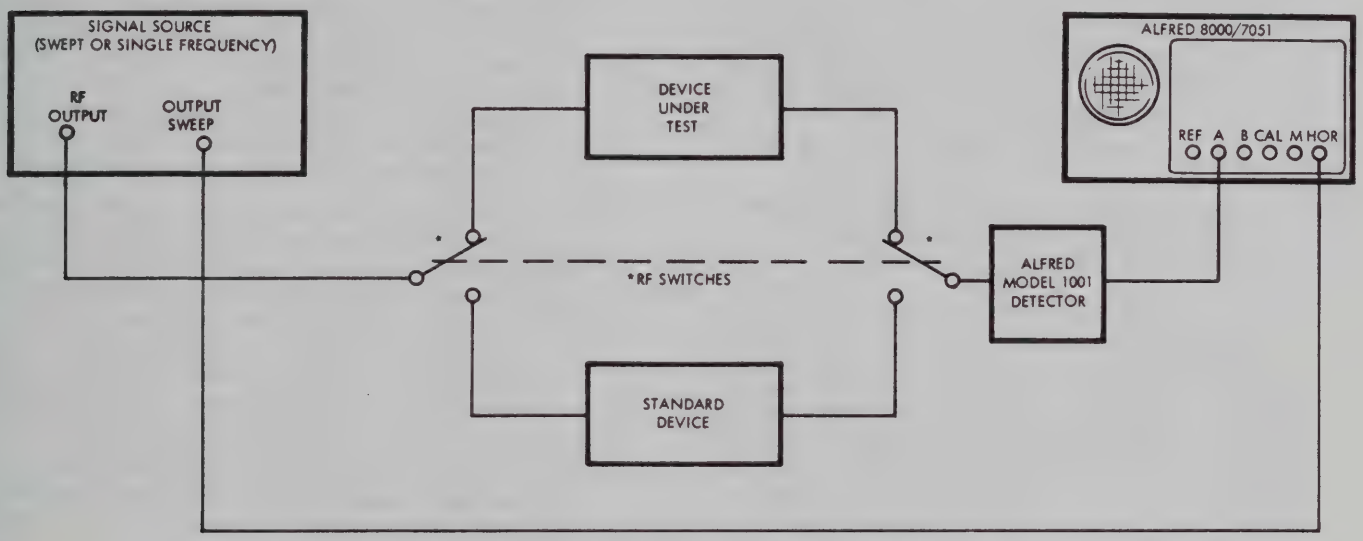
3.13.7 USE OF THE MODEL 8000/7051 FOR READOUT OF RF COMPARISON-TYPE MEASUREMENTS.

The high sensitivity of the Model 8000/7051 ($\approx$20 μv/cm maximum) makes it an ideal readout indicator device for rf comparison measurement techniques, using bridge or dual-path test circuits. For such measurements, the instrument should be operated in the LOG presentation mode, following the procedure given in Par. 3.8 for absolute level measurements. The detector driven by the bridge or dual-path comparison circuit is then connected to Channel A or B. When a packaged bridge/detector such as the Telonic Rho-Tector is used, the CRT presentation can be calibrated by substituting a known standard for the device under test, and calibration accuracy is determined by the accuracy of these standards. When the test set-up is a dual-path or bridge circuit using an external detector, the use of an ALFRED Model 1001 Crystal Detector permits direct readout in db or dbm over a 60 db range.

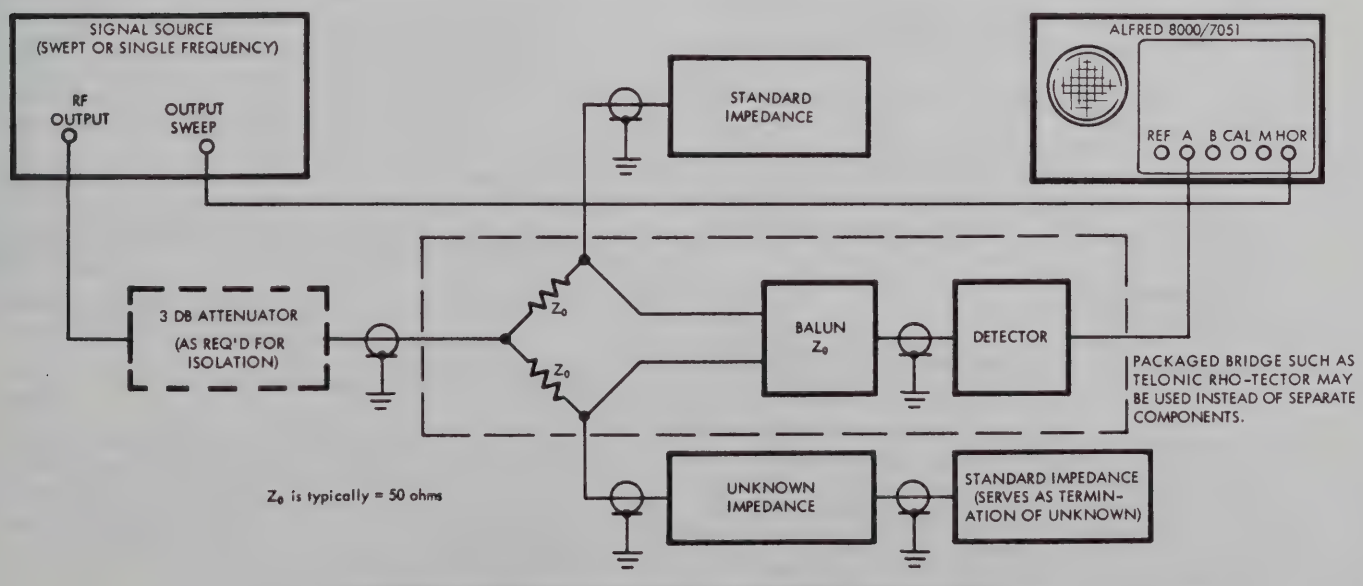
For measurement of transmission gain or loss, the test set-up of Fig. 3-18A is convenient. The Model 8000/7051 display is calibrated to the zero-set line with the test path switched through the variable standard. The performance of the device under test is then monitored, and the difference in performance between the standard and the unknown can be read directly in db at any point in the sweep from the display. If desired, the VERTICAL POSITION digital counters can be set for direct dbm readout to evaluate the device power output levels in absolute terms.

For measurement of impedance by means of reflection characteristics, the symmetrical bridge set-up shown in Figure 3-18B may be used. Two legs of the bridge are provided by external impedances, one a "standard" impedance termination and the other being the unknown impedance terminated by a "standard". The Model 8000/7051 display is calibrated by substituting terminations of known VSWR for the unknown impedance. The performance of the unknown can then be evaluated in terms of the known-VSWR calibration curves.

Note that Channels A and B can be used for reading out two test set-ups simultaneously if desired.



A. MEASUREMENT OF TRANSMISSION CHARACTERISTICS USING DUAL-PATH COMPARISON CIRCUIT



B. MEASUREMENT OF REFLECTION CHARACTERISTICS USING BRIDGE COMPARISON CIRCUIT

FIGURE 3-18. TYPICAL TEST CONNECTIONS FOR COMPARISON-TYPE MEASUREMENT TECHNIQUES.

3.13.8 SOURCE OUTPUT VSWR MEASUREMENT. Output VSWR on microwave signal generators, sweep oscillators, and amplifiers can be measured using the test set-up of Figure 3-19. This test arrangement uses the device under test to supply the test signal so that additional test sources are not required. The circuit is essentially a set-up for absolute power level measurement (LOG A CHN Mode), but since only the relative response under various conditions of reflection is to be measured, the digital counters need not be calibrated for absolute power readout.

The test set-up shown in Figure 3-19 does not include an external leveling loop, and is suitable for testing the basic source match of a signal generator or unleveled sweeper. To check the effectiveness of sweeper leveling in improving the source match, the sweeper may be operated in an internally leveled mode, or an additional output forward coupler may be added between the rf output connection and the test signal output coupler to es- - tablish at-the-load leveling.

The test procedure when measuring swept sources utilizes a moving short to reflect ≈ 100% of the device output power back to the source. If the source match is perfect (VSWR 1.0:1), all reflected power will be absorbed and the resultant power coupled into the forward-oriented test output coupler will not vary with the position of the moving short. When source mismatch is present, a corresponding portion of the reflected power will be re-reflected in the forward direction, and, as the position of the short is moved, this power will alternately add to or subtract from the power provided by the tube itself.

For any particular frequency, one setting of the moving short will cause all reflections to be in-phase with the source output, producing a maximum output level noticeably greater than the normal forward power coupled out when the transmission path is terminated in a matched load. A different setting of the moving short will cause alternate reflections to be out-of-phase with the source output, producing a minimum output level lower than the normal forward power coupled out into a matched load.

NOTE: If output VSWR performance working into a particular known mismatch load is desired, an attenuator with a value of half the effective return loss of such a mismatch load may be connected between the directional coupler output and the sliding short.

For measurements of single-frequency sources or swept sources, the readout can be interpreted directly from the CRT display excursion limits without calibrating with a matched load or drawing "calibration bands" corresponding to various VSWR values on the graticule. For "go/no go" testing, however, it may be desirable to perform such calibration.

Alternate procedures for measurements with and without graticule calibration lines are given below:

A. Procedure for Direct Measurement Without Graticule Calibration Lines.

a. Make connections as shown in Figure 3-19, using the sliding short at the output of the test signal coupler.

b. Make the following control settings on the Model 8000/7051:

DISPLAY Mode Selector to LOG A CHN
VERTICAL SENSITIVITY to 0.5 DB/DIV
HORIZONTAL POSITION Controls, BALANCE Control switch } set in accordance with the signal source and display sweep mode used; see Paragraph 3.7

c. Operate the device under test in the single frequency(ies) or swept band of interest.

d. At each single frequency, or at the frequency where maximum excursion occurs within any swept band, move the sliding short through its limit of travel and then position it at the setting which drives the trace to its lowest point.

e. Turn the red A CHANNEL VERTICAL POSITION knob until the lowest point on the trace obtained in d is moved to the graticule centerline. Turn the black knob CW to the PRESET position, and turn the red knob to set the A CHANNEL digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position.

f. While continuing to operate at the same single frequency or in the same frequency band, move the sliding short through its limit of travel again, and then position it at the point which drives the trace to its highest point at the same frequency at which the excursion of step d was measured.

g. Turn the red A CHANNEL VERTICAL POSITION knob until the highest point on the trace obtained in f is moved to the graticule centerline. The A CHANNEL GAIN DB counter reading is the direct db equivalent of the numerical VSWR ratio. The VSWR may be obtained directly from any voltage db nomograph including the ALFRED NOMOGRAPH slide rule, or the following equation:

$$\text{VSWR} = \text{Antilog}_{10} \frac{(\text{GAIN DB reading})}{20}$$

Examples: If GAIN DB reading is 6.02, VSWR is 2.0:1
If GAIN DB reading is 9.54, VSWR is 3.0:1
If GAIN DB reading is 3.52, VSWR is 1.5:1

NOTE: If it is desired to read VSWR visually from the CRT presentation without using the digital counters or calibrating the graticule, the total graticule distance between the excursion limits of the trace at the same frequency in steps d and f above may be evaluated directly in db with a suitable VERTICAL SENSITIVITY setting by "counting squares". Then convert the resultant db value to VSWR by the above method.

B. Procedure for Measurement Readout Based on Graticule Calibration Lines.

a. Make connections as shown in Figure 3-19, using the matched non-reflecting load at the output of the test signal coupler.

b. Make the following control settings on the Model 8000/7051:

DISPLAY Mode Selector to LOG A CHN
VERTICAL SENSITIVITY to 2.0 DB/DIV
HORIZONTAL POSITION Controls, BALANCE Control switch } set in accordance with the signal source and display sweep mode used; see Paragraph 3.7

c. Operate the device under test in the single frequency(ies) or swept band of interest.

d. Turn the red A CHANNEL VERTICAL POSITION knob until the midpoint of the vertical trace excursion is positioned on the graticule centerline. Turn the black knob CW, to the PRESET position, and turn the red knob to set the A CHANNEL digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position. (The resultant graticule trace corresponds to 1.0:1 VSWR, and may be so marked if desired.)

e. Select from Figure 3-20, a trace upward excursion limit in db corresponding to a limiting VSWR value (or other VSWR values as desired for detailed calibration). Turn the red A CHANNEL VERTICAL POSITION knob CW to raise the trace until the selected db reading appears in the DB LOSS window. Mark this trace on the graticule (or on a transparent acetate overlay) and label with the corresponding VSWR value. Repeat for other calibration traces as desired in the upper sector of the graticule.

f. Select from Figure 3-20, the trace downward excursion limit in db corresponding to the same limiting and/or calibration VSWR values used in step e. Turn the red A CHANNEL VERTICAL POSITION knob CW to lower the trace until the selected db reading appears in the DB GAIN window. Mark this trace on the graticule or overlay and label with the corresponding VSWR value. Repeat for other calibration traces as desired in the lower sector of the graticule.

g. Remove the non-reflecting load and connect the sliding short at the output of the test signal coupler.

h. Turn the red A CHANNEL VERTICAL POSITION control until the counter reads 00.0.

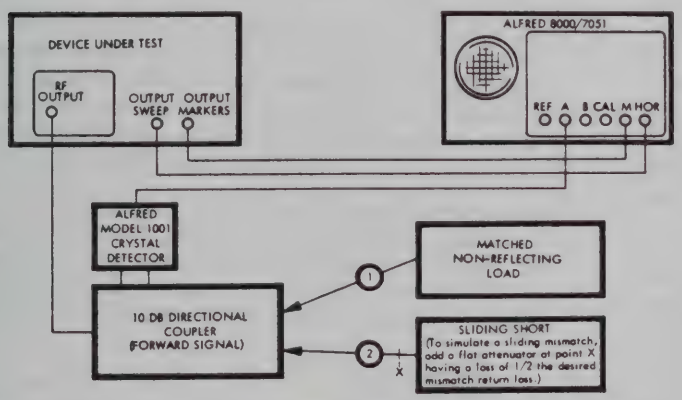

DEVICE UNDER TEST
RF OUTPUT
OUTPUT SWEEP
OUTPUT MARKERS
ALFRED 8000/7051
REF A B CAL M HOR
ALFRED MODEL 1001 CRYSTAL DETECTOR
MATCHED NON-REFLECTING LOAD
10 DB DIRECTIONAL COUPLER (FORWARD SIGNAL)
SLIDING SHORT
(To simulate a sliding mismatch, add a flat attenuator at point X having a loss of 1/2 the desired mismatch return loss.)
1
2
X

FIGURE 3-19. TYPICAL TEST CONNECTIONS FOR MEASUREMENT OF SOURCE OUTPUT VSWR

i. Move the sliding short through its limit of travel and note the upper and lower extremes of the trace excursion with respect to the graticule calibration or limit lines. The maximum effective output VSWR can be read from the trace position with respect to these calibration lines. There should be reasonable agreement between the readout obtained in the two sectors of the graticule, from the trace excursion limits on either side of the 1.0:1 VSWR centerline.

C. Sources of Error.

a. Obviously, the coupler directivity will affect the measurement accuracy. Refer to paragraph 3.14 for a detailed discussion of directivity error and other accuracy considerations.

b. The definition of "hot" VSWR when measuring microwave oscillator performance is not clearly specified throughout the industry. Presence of considerable reflected power in the rf output line when the sliding short termination is used can produce erratic output performance from the oscillator tube which will not appear when working into any reasonably matched load. Measurements made with a sliding short test circuit to determine the reflection coefficient of the source will indicate a greater VSWR than "working VSWR" measurements made with a standard sliding mismatch (consisting of, for example, a 3 db attenuator in series with a sliding short to constitute a sliding mismatch of 3:1 VSWR). However, if the "working VSWR" obtained from the measurement with a sliding mismatch is interpreted as

$$VSWR = \frac{1 + [\rho_S \cdot \rho_L]}{1 - [\rho_S \cdot \rho_L]}$$

where ρ_S = Source reflection coefficient

ρ_L = Load mismatch reflection coefficient

Then the resultant value for ρ_S should approximately agree with the ρ_S determined with the sliding short VSWR measurement (where $\rho_L = 1$).

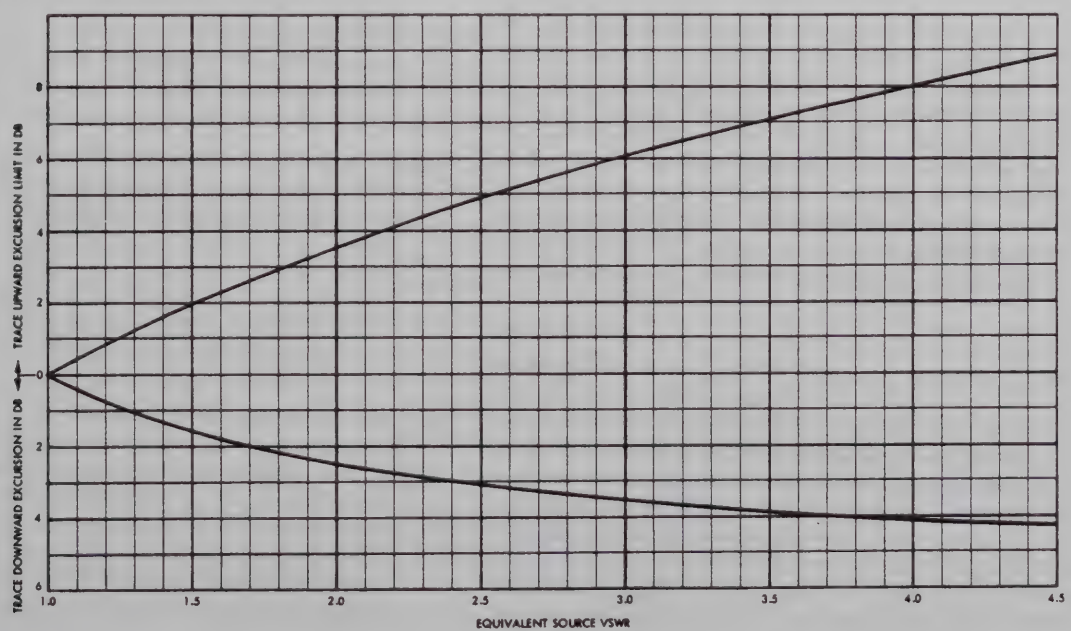


FIGURE 3-20. TRACE EXCURSION LIMITS vs. EQUIVALENT VSWR, FOR CALIBRATION OR READOUT OF SOURCE OUTPUT VSWR TESTS

3.14 MEASUREMENT ACCURACY CONSIDERATIONS.

3.14.1 SOURCES OF ERROR IN REFLECTOMETER MEASUREMENTS.

A determination of the total significant error in return loss measurements requires a summation of the error due to mainline SWR, coupler directivities, coupler tracking, and the Model 8000/7051 instrumentation accuracy. The most useful expression of total error is a + and a - db error term which can be used as an uncertainty factor for the direct db readout. The four contributions to this error expression can be determined as follows:

a. Model 8000/7051 instrumentation error: determine from instrument db error specification given in (1) below.

b. Error due to imperfect frequency response and/or imperfect frequency response tracking of directional couplers and other components in the external test loop: determine from the calibration display on the CRT as described in (2) below.

c. Error due to the imperfect directivity of directional couplers used in the external test loop: determine directly in + and - db from Fig. 3-21 or from ALFRED NOMOGRAPH Slide Rule.

d. Error due to the existence of some amount of mainline VSWR in the directional couplers used in the external test loop: determine directly in + and - db from Fig. 3-22.

NOTE: Error categories b, c, and d above are errors in external components which will have the same values regardless of the measurement technique used, except that in other systems requiring use of an external precision attenuator, the error of that component will be added to the errors present in measurements with the ALFRED Model 8000/7051.

Once the limits of error in the db return loss reading have been determined, the corresponding error in reflection coefficient (ρ) and VSWR can be determined by using the maximum and minimum limiting db readings with standard nomograph tables, the ALFRED NOMOGRAPH Slide Rule, or the general formulas given below:

$$\text{Return loss (db)} = -20 \log |\rho| \qquad \text{VSWR} = \frac{1 + |\rho|}{1 - |\rho|}$$

1. Instrument Error. When using the 8000/7051 measurement system to measure the variation in a signal level by the calibrated offset method, i.e. with readout on the VERTICAL POSITION offset digital counters, the basic accuracy of the instrument is 2% of the db reading or 0.4 db, whichever is greatest. Thus, for example, measurement of a signal variation of 30 db by the calibrated offset method would yield an error not greater than ± .6 db.

This accuracy includes error in the instrument correction of the crystal detector output departure from square law over a 60-db dynamic range. The specification of maximum error in db is most convenient because the instrument reads directly in db. In most reflectometer measurements the error due to the external components will significantly exceed the ALFRED Model 8000/7051 error. The 2% instrumentation accuracy of the Model 8000/7051 is comparable to or better than the instrumentation accuracy of conventional ratiometers.

2. Frequency Tracking Error. In ratiometric level measurements for determination of transmission gain and loss or for return loss, the imperfect frequency response characteristics of couplers used for incident, reflected, and transmitted power sampling will cancel out if the couplers have identical characteristics. Normally the Model 8000/7051 is used with directional couplers and crystal detectors (such as the Model 1403) which are closely matched in frequency response. Tracking error, therefore, will amount to a few tenths of a db or less.

The amount of measurement error due to poor coupler tracking can be directly measured at the time zero-set calibration for ratiometric readout is performed. Couplers with tracking error (and crystal detectors with non-identical frequency response error) will produce a non-flat calibration line on the CRT when the device under test is bypassed for transmission performance calibration purposes, or when the reflected power coupler output is shorted for return loss calibration purposes. With high-directivity couplers, the deviation of these two calibration lines from horizontal, evaluated in db in accordance with the CRT calibration sensitivity being used, gives the readout correction factor in db vs. frequency (horizontal position) that must be applied to all measurements.

The flexible Offset controls allow the non-horizontal trace to be adjusted tangent to the desired graticule line under calibration conditions, so that all correction increments will have the same algebraic sign, for simplicity. Such a correction trace can be marked with grease pencil on the graticule for ease in applying the correction factors to subsequent measurements. For gain measurements, set the trace tangent to the zero line so that all deviations drop below the line, and add the db correction to the subsequent measurement readout; for loss measurements, set the trace tangent to the zero line so that all deviations go above the line, and again add the db correction to the subsequent readout.

NOTE: In test set-ups using directional couplers, the vector addition of all signals reaching the coupler arm will produce a "ripple" in the broadband zero-set calibration line as the phase of the signal components shifts from mutually aiding to opposing during the sweep. The extraneous signals producing this effect result from directivity error in the coupler itself (which admits a portion of the reverse signal into the forward coupling arm). The true directivity error effects in the measurement, where the actual locations of directivity peak-and-valley ripples are unknown because of complex impedance effects, can be assessed only by the limits given in Figure 3-21 (see #3 below). Therefore, it is useful, particularly with low directivity couplers, to separate the display "ripple" due to directivity error from that due to tracking, so that only the latter is "calibrated out" by means of the zero-set correction line described above. If the transmitted power coupler is properly terminated, the directivity-ripple should only appear in the reflected power ratio measurement.

This directivity error ripple can be separated from the non-horizontal trace characteristics due to tracking error in coaxial systems by obtaining a reflected power calibration trace with the output port of the reflected power coupler first shorted and then open-circuited. When this is done, the peaks and valleys of the directivity error ripple will reverse, while any non-flatness in the calibration trace due to tracking error will remain unaffected. The tracking error calibration line can then be drawn to bisect the peak-and-valley excursions of the directivity error ripple. Since the open circuit is not a perfect infinite-impedance termination, this correction procedure is approximate.

In waveguide systems, and for more accurate results in separating out the directivity error ripple in coaxial systems, a sliding termination should be connected to the output port of the device under test, in place of the transmitted power coupler. Then with the test set-up operated for single-frequency measurement, adjustment of the sliding termination will produce a vertical displacement in the display position. If the test set-up is operated in a swept mode, adjustment of the sliding termination will cause a ripple to move along the display trace. The tracking error calibration line should then be drawn to bisect the peak-to-peak excursion thus measured at each frequency. The

peak-to-peak amplitude of this ripple then represents the maximum display error due to output reflections adding to the power reflected at the device input.

3. Coupler Directivity Error. When measuring small values of VSWR (< 3 to 1) with a reflectometer system, the principal source of error is the imperfect directivity of the directional coupler sampling the reflected wave. As the mismatch being measured becomes larger, the relative error due to the effects of mainline VSWR becomes greater.

Figure 3-21 shows the maximum error in measured return loss as a function of actual return loss for couplers having various directivity values. The curves of Figure 3-21 take into consideration error due to imperfect directivity in both the incident and reflected wave sampling couplers, and assume that the directivity values of each are equal. The calculations for Figure 3-21 are given on page 3-27.

NOTE: The ALFRED Model 1003 Crystal Detector is available for measurement and detection applications involving components and systems having Amphenol precision connectors. The Model 1003, with a precision rf input connector, meets the same high-performance specifications as the Model 1001. The Model 1003 can link new precision reflectometer bridges and dual directional couplers directly to the Model 8000/7051 Sweep Network Analyzer. Since the Model 1003 connects directly to high-directivity reflectometer bridges and directional couplers having precision connectors, without requiring adapters, the directivity error normally produced by components with standard Type N connectors is eliminated.

4. Mainline VSWR Error. Many discussions of reflectometer measurement error consider only the error due to imperfect directivity of the reverse coupler. The error due to directional coupler mainline VSWR is usually ignored because when measuring a component with good match, it is considerably less than that due to imperfect directivity.

Figure 3-22 shows the maximum error in measured return loss as a function of mainline VSWR of the coupler. The calculations for the curves shown in Figure 3-22 are given on page 3-27.

NOTE: As an example, if it is desired to measure the return loss of a device having a VSWR of 1.2 with a coupler having a directivity of 30 db and a mainline VSWR of 1.15, the db error due to the directivity will be about 6.2 times the db error due to the mainline VSWR, and will be about 9 times the instrument error. Measuring the same match using a coupler having a directivity of 40 db, the error due to the directivity will be 2.6 times the error due to the basic instrument. The reflectometer technique theoretically has excellent accuracy over a wide VSWR range with a coupler having 40 db directivity. The lowest VSWR that can accurately be measured is limited by the directivity of the reflected power readout coupler.

3.14.2 SOURCES OF ERROR IN TRANSMISSION GAIN/LOSS RATIO MEASUREMENTS.

The significant sources of error in transmission performance ratio measurements are those in categories a and b discussed in the reflectometer measurement error analysis above. Errors discussed under categories c and d can be neglected except where significant VSWR exists in the output (transmission response sampler) end of the external test loop. Excessive VSWR levels can be avoided by using quality directional couplers and terminating the transmission response coupler with a well-matched termination.

The instrumentation error and frequency tracking error for any db readout can be evaluated in accordance with the above analysis.

3.14.3 SOURCES OF ERROR IN ABSOLUTE LEVEL MEASUREMENTS.

The significant sources of error when making absolute level measurements with the ALFRED Model 8000/7051 Sweep Network Analyzer System can be considered in three categories which are discussed in detail below. These categories are:

a. Error due to the instrument (Model 8000/7051).

b. Error due to improper calibration signal level.

c. Frequency response error in the crystal detector between the reference and measurement frequency.

1. Instrument Error. When used to measure absolute power, the accuracy of the instrument is equal to 2% of the db differential reading above or below the reference level at which the VERTICAL POSITION Offset digital counters were calibrated, or 0.4 db, whichever is greatest.

2. Internal Calibrator Signal Error. The OUTPUT CALIBRATOR signal has an absolute error of less than ± 0.3 db at +20 DBM, and less than ± 0.6 db at all other CALIBRATOR DBM settings. The relative error between any combination of CALIBRATOR DBM settings is less than ± 0.3 dbm.

3. Crystal Detector Frequency Response Error. The frequency response error of the ALFRED Model 1001 Crystal Detector is typically less than ± 0.2 db from the OUTPUT CALIBRATOR frequency of 30 MHz, to 8 GHz, and does not exceed ± 0.5 db through X-band (< 12.4 GHz).

4. Determination of Total Error in Absolute Power Measurements. A determination of total error in absolute power measurements requires a summation of the error due to crystal detector frequency response, rf calibrator signal inaccuracy, and the Model 8000/7051 instrumentation accuracy. The most useful expression of total error is a + and a - db error term which can be used as an uncertainty factor for the direct db readout. The three contributions to this error expression can be determined as follows:

a. Model 8000/7051 instrumentation error: Determine from instrument db error specification given in (1) above.

b. Calibration Signal Level Error: If the Model 8000/7051 internal rf calibrator is used, determine from its absolute error specification given in (2) above. If another rf calibration source is used, determine its error from specification or calibration data.

c. Crystal Detector Frequency Response Error: Determine from specification or calibration data for the detector being used.

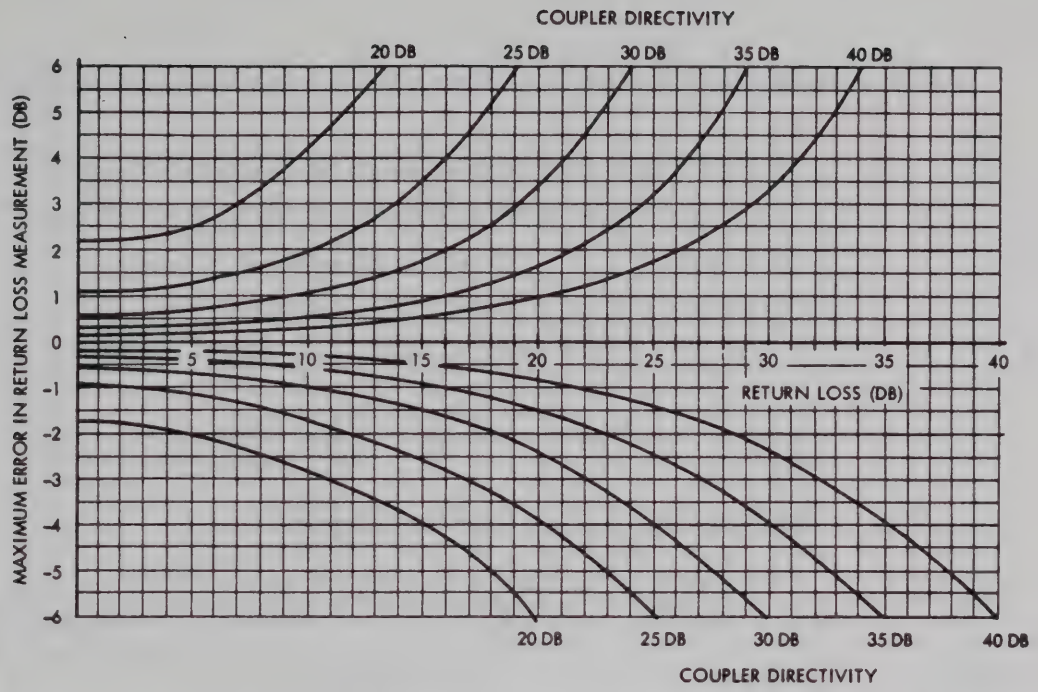


FIGURE 3-21. MAXIMUM + AND – DB ERROR IN RETURN LOSS MEASUREMENTS DUE TO COUPLER DIRECTIVITY EFFECTS, VS. INDICATED RETURN LOSS, FOR VARIOUS COUPLER DIRECTIVITY VALUES.

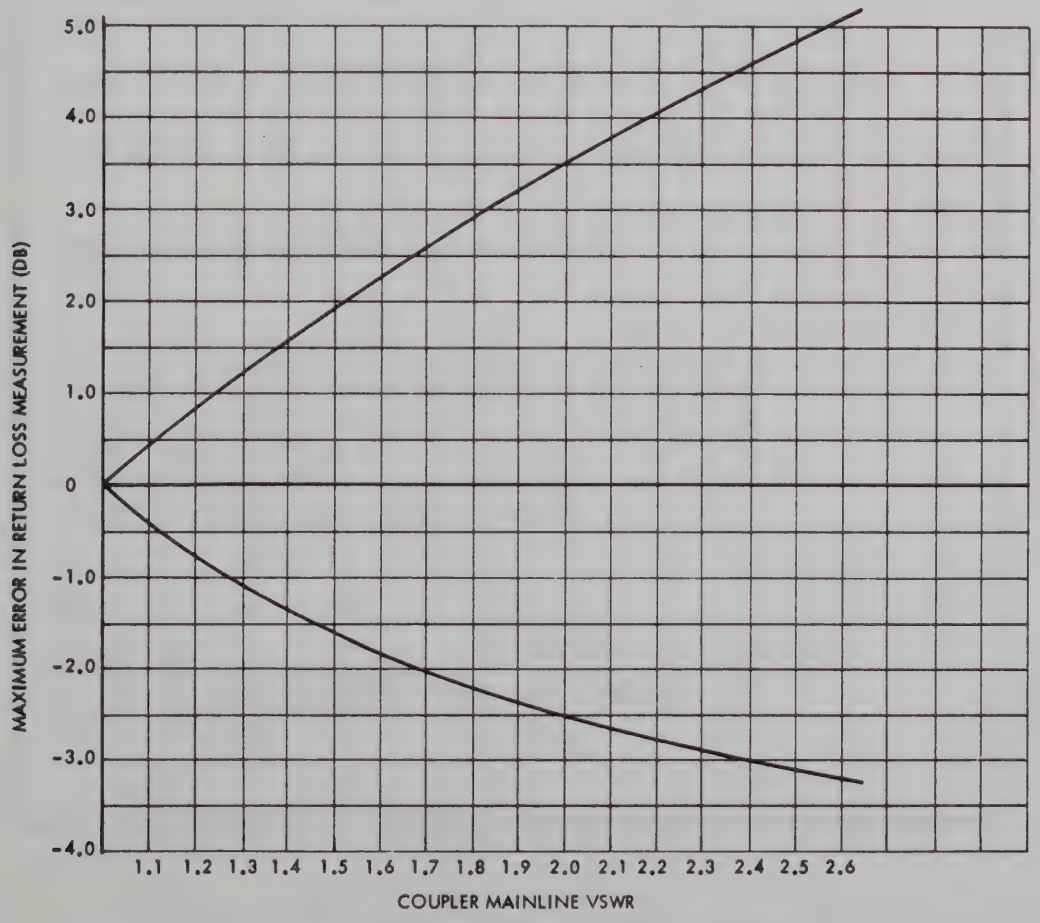


FIGURE 3-22. MAXIMUM + AND – DB ERROR IN RETURN LOSS MEASUREMENTS DUE TO MAINLINE VSWR EFFECTS.

DERIVATION OF ERROR ANALYSIS CURVES

Error in Reflection Measurements Due to Coupler Directivity (Figure 3-21).

E_{REV} = Voltage output from reverse (reflected) power coupler = $[\rho_L E_{in} \pm D E_{in}]K$ (1)

where ρ_L = load reflection coefficient; E_{in} = input voltage; D = coupler directivity; K = coupling factor

E_{INC} = Voltage output from incident power coupler = $[E_{in} \pm \rho_L E_{in} D]\ K$ (2)

$$\rho_{measured} = \rho_M = \frac{E_{REV}}{E_{INC}} = \frac{\rho_L \pm D}{1 \pm \rho_L D}$$ (assuming both couplers have same K and D) (3)

$$= \frac{\rho_L \pm D}{1 - \rho_L D}$$ (for maximum deviation of either polarity) (4)

$$\rho_{\substack{error \\ increment \\ (max.\ positive)}} = \rho_M - \rho_L = \frac{\rho_L + D}{1 - \rho_L D} - \rho_L = \frac{\rho_L + D - \rho_L + \rho_L^2 D}{1 - \rho_L D} = \frac{D(1 + \rho_L^2)}{1 - \rho_L D}$$ (5)

and

$$\rho_{\substack{error \\ increment \\ (max.\ negative)}} = \frac{D(1 - \rho_L^2)}{1 - \rho_L D}$$ (6)

$$\text{db readout} = -20 \log \rho_M = -20 \log (\rho_L + \rho_{error}) = -20 \log \rho_L \left(1 + \frac{\rho_{error}}{\rho_L}\right)$$ (7)

$$\text{db error} = -20 \log \rho_L \left(1 + \frac{\rho_{error}}{\rho_L}\right) - 20 \log \rho_L = -20 \log \left(1 + \frac{\rho_{error}}{\rho_L}\right)$$ (8)

$$\text{Max + error (db)} = -20 \log \frac{1 + D(1 + \rho_L^2)}{1 - \rho_L D}; \quad \text{max - error (db)} = -20 \log \frac{1 + D(1 - \rho_L^2)}{1 - \rho_L D}$$

These are the equations used to plot Figure 3-21. (9,10)

A handy approximation for VSWR values less than 3 to 1 (return loss < 6 db) is:

$$\rho_{\substack{error \\ increment}} = \pm D(1 + \rho_L^2)$$ (11)

Error in Reflection Measurements Due to Mainline VSWR (Figure 3-22).

The portion of the reflected signal "robbed" from the reflected power coupler because of reflection at the coupler primary output port, due to mainline VSWR, is given by $(E_{in} \rho_L \rho_{ML})$; where ρ_{ML} = reflection coefficient of reflected power coupler. Therefore: (12)

$$\rho_{measured} = \rho_L \pm \rho_L \rho_{ML} = \rho_L (1 \pm \rho_{ML})$$ (13)

$$\text{indicated Return Loss} = -20 \log \rho_L - 20 \log (1 \pm \rho_{ML})$$ (14)

db error = $-20 \log (1 \pm \rho_{ML})$. This is the equation used to plot Figure 3-22. (15)

A convenient expression of mainline VSWR error in terms of the reflection coefficient is as follows:

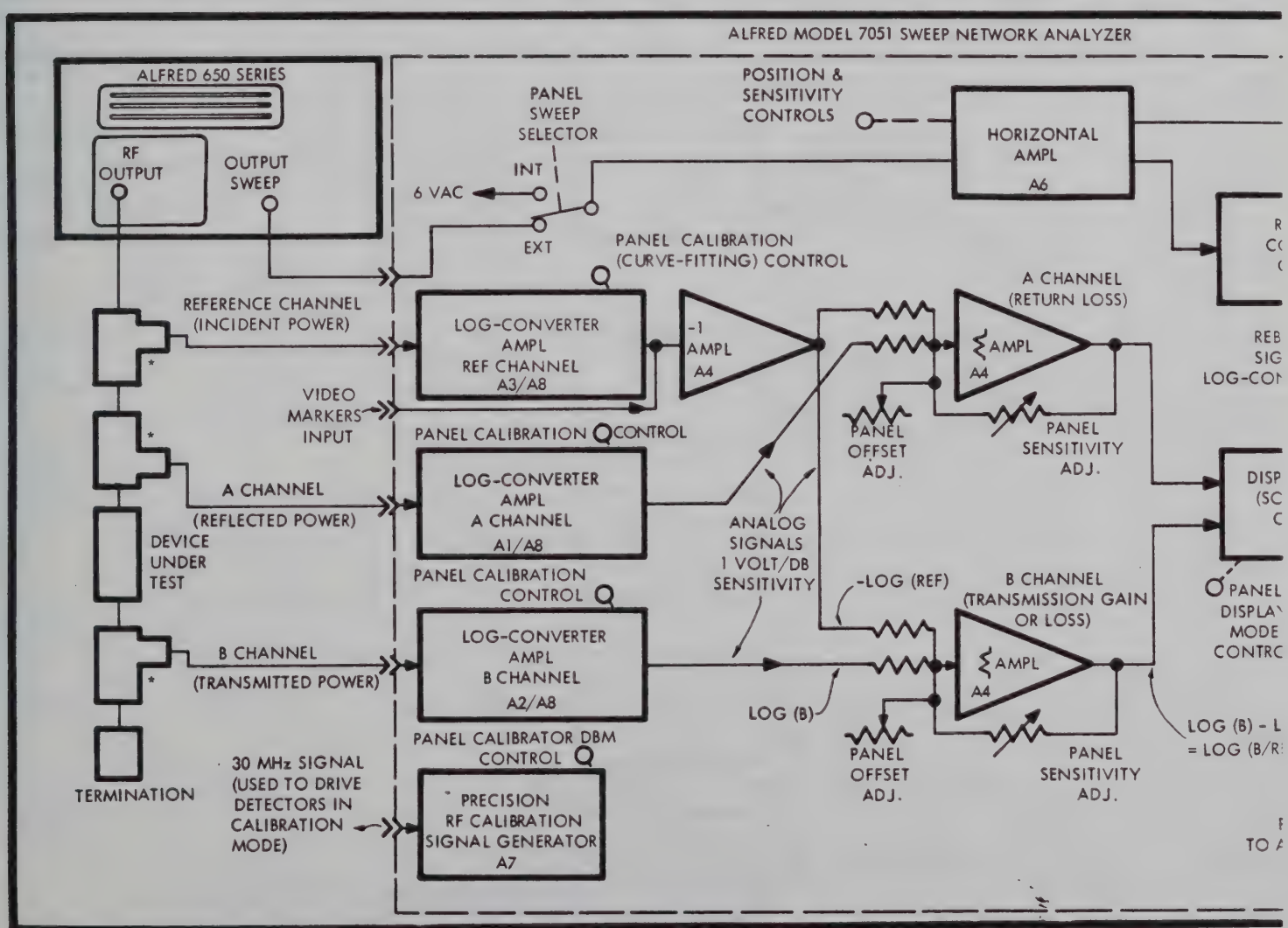
$$\rho_{\substack{error \\ increment}} = \pm \rho_L \rho_{ML}$$ (16)

4.1 BLOCK DIAGRAM DESCRIPTION (See Figure 4-1).

4.1.1 GENERAL. A simplified block diagram of the 8000/7051 measurement system and a typical rf test circuit is shown in Figure 4-1. The circuit arrangement in both the Oscilloscope and the Sweep Network Analyzer Plug-in Unit are shown. The test circuit includes samplers to detect incident, reflected, and transmitted power in the circuit of the device under test. Any three points, as desired, can be used for ratio measurements, and any two points can be used for absolute level measurements.

The capability of measuring ratio eliminates the need for leveling the rf source. The use of self-balancing state-of-the-art solid-state dc amplifiers in the measurement system permits handling a 60-db range without requiring the source to be modulated. The PC Boards and functional modules and their functions are tabulated in Table 4-1 for general reference. The block diagram carries reference designators which indicate the module or PC board(s) performing each function. Signal paths are indicated on the schematic diagrams for Board, which are included in Section 7 in module-designator order (see indexing in Table 4-1 and on These schematics are printed with blank aprons and folded out for reference while reading this section.

4.1.2 SWEEP NETWORK ANALYZER. As shown 4-1, the output of each crystal detector is applied verter amplifier. The output of each log converter arithmic representation of its input signal and has of approximately 1 V/db. The output of the refere verter amplifier is applied to an inversion amplifie computation techniques are employed to obtain the ratios. For example, referring to the block diagram the Channel B Summing Amplifier are Log B and - output of the Channel B Summing Amplifier is dire tional to (log B -log Ref.), which equals log (B/Re brated dc offset is injected at the input of each su fier. Note that the display sensitivity of each cha



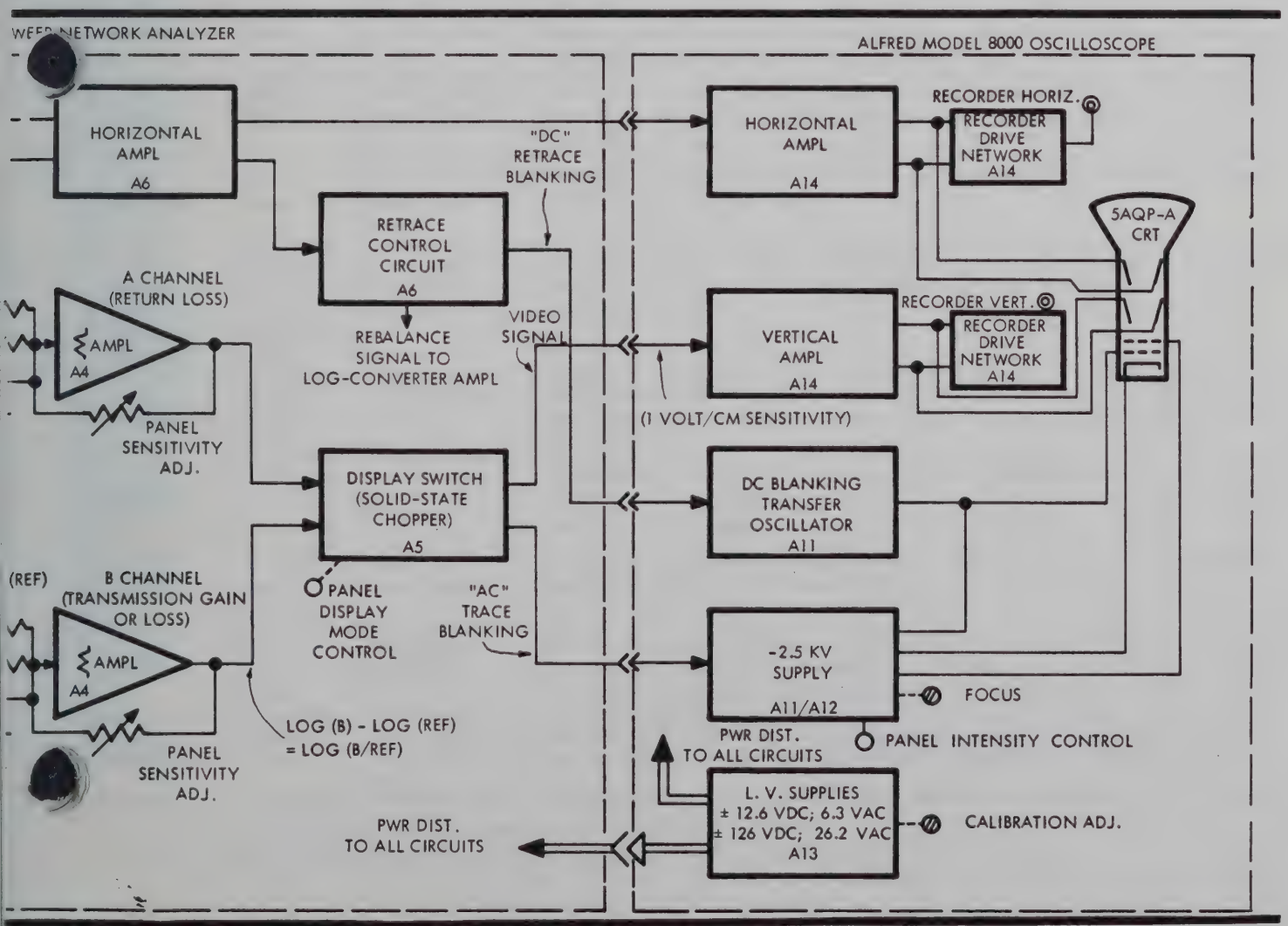
* ALFRED RF SAMPLERS OR DIRECTIONAL COUPLERS WITH STANDARD CRYSTAL DETECTORS

FIGURE 4-1. BLOCK DIAGRAM OF 8000/7051 AND TYPI

indicated on the schematic diagrams for each PC hich are included in Section 7 in module-reference- or order (see indexing in Table 4-1 and on page 7-0). ematics are printed with blank aprons and can be ut for reference while reading this section.

WEEP NETWORK ANALYZER. As shown in Figure output of each crystal detector is applied to a log con- nplifier. The output of each log converter is a log- representation of its input signal and has a sensitivity ximately 1 V/db. The output of the reference log con- nplifier is applied to an inversion amplifier. Analog tion techniques are employed to obtain the desired For example, referring to the block diagram, inputs to nel B Summing Amplifier are Log B and -log Ref. The f the Channel B Summing Amplifier is directly propor- (log B -log Ref.), which equals log (B/Ref.). The cali- c offset is injected at the input of each summing ampli- ote that the display sensitivity of each channel is varied by varying the feedback resistor around the summing amplifier in that channel. When it is not desired to measure the ratio of the A or B Channel signal to the reference Channel signal, the output of the reference Channel log converter amplifier is merely not applied to the summing amplifier in each channel. This permits readout of the absolute level of the signal applied to the A and B Channels, when the display has been calibrated in terms of detector response to known-level signals from the built-in calibrator. Outputs from the summing amplifiers are applied to the display switch which allows the channel outputs to be displayed singly or simultaneously. The output of the display switch drives the main vertical amplifier in the Model 8000 Oscilloscope.

The Horizontal signal from the swept source is applied to the Model 7051. Circuitry in the 7051 generates the retrace blanking signal for the display and provides for the adjustment of the horizontal presentation. Retrace blanking is generated for sweep signals having retrace times as slow as 100 msec.

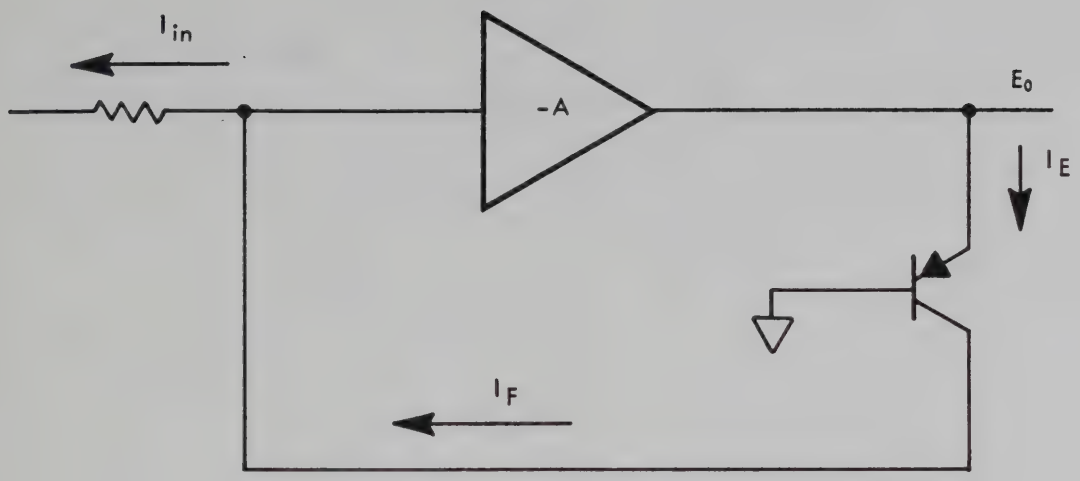


CK DIAGRAM OF 8000/7051 AND TYPICAL RF TEST CIRCUIT

Table 4-1. Printed Circuit Cards and Modules in the Model 8000/7051 System

PC Card or Module Ref Des. & (Sect. 7 Schematic)	Name	Location	Description
A1 (900824C)	A Channel Amplifier*	Top of Model 7051 Plug-in	Accepts the output signal from the A Channel crystal detector. Provides true logarithmic conversion of crystal detector output and compensation for crystal deviation from square law performance,and amplification as required, to develop an output of 1 volt/db over a 60-db dynamic range.
A2 (900824C)	B Channel Amplifier*	Top of Model 7051 Plug-in	Accepts the output signal from the B Channel crystal detector. Physically and functionally identical to A1.
A3 (900824C)	REF Chn Amplifier*	Top of Model 7051 Plug-in	Accepts the output signal from the REF Channel crystal detector. Physically and functionally identical to A1.
A4 (900825C)	Summing Amplifier	Top of Model 7051 Plug-in	Contains two summing operational amplifiers that accept the outputs of A1, A2, and A3 in various combinations according to operating mode. Provides A/REF and B/REF ratio readout by subtraction of logarithmic voltages, or direct logarithmic voltage readout of A and/or B. Provides display sensitivity control through adjustment of amplifier feedback, and display offset adjustment through summation of a voltage supplied by the VERTICAL POSITION controls.
A5 (900826C)	Chopping Circuit	Top of Model 7051 Plug-in	Accepts the output of the two summing amplifiers contained in A4, and provides an output according to the selected operating mode: chopped dual-channel output or single-channel continuous output. Output level is 1 volt/cm of CRT deflection.
A6 (900827D)	Sweep Circuit	Top of Model 7051 Plug-in	Operation depends upon horizontal deflection mode desired. Generates internal sweep or amplifies externally-supplied horizontal deflection voltage. Permits amplification adjustment and horizontal position control.
A7 (900823D)	Calibrator PC Board	Behind panel of Model 7051 Plug-in	Develops 30 MHz rf calibration signal with a level of +20 dbm, which drives the attenuator operated by the CALIBRATOR switch to provide precision output levels in 10-db steps down to -40 dbm.
A8 (900823D)	Oven Assembly	Bottom of Model 7051 Plug-in	Provides regulated thermal environment for transistors in low-level circuits associated with A1, A2, and A3.
A9 Mechanical except for R8 and R9 M900823D	VERTICAL POSITION Offset controls & digital counter	Front Panel of Model 7051 Plug-in	Provides electronic offset up to 60 db of either gain or loss, indicated with 0.1-db resolution on 3-digit counters which are settable for calibration at any indication from 00.0 to 99.9.
A11 (900807C)	HV Reg & Blanking Circuit	Rear of Model 8000	Regulates the high voltage supply which drives the CRT electron gun; and couples the dc blanking signal with appropriate amplification to drive the CRT grid bias circuit of A12.
A12 (900804D)	HV Rectifier Circuit	Rear of Model 8000 inside shield	Rectifies the high voltage generated by the high voltage supply, and provides suitable filtering and decoupling to drive the various CRT electrodes and supply feedback to the HV regulator circuit.
A13 (900805C)	LV Power Supply Circuit	Center of Model 8000	Generates regulated low voltage power used by all other circuits in the 8000/7051. Supplies -12.6 V, +12.6 V, and +126 V.
A14 (900806C)	CRT Deflection Circuit	Left side of Model 8000	Provides impedance conversion amplification for the vertical and horizontal deflection signals supplied by the Model 7051. Furnishes output signals to drive the CRT deflection plates and the off-scale indicator lamp quadrant.
A15 (900823D)	Calibrator Assembly	Behind panel of Model 7051 Plug-in	Includes A7 Calibrator PC Board (see above) and CALIBRATOR attenuator switch which provides precision output levels in 10-db steps from +20 dbm to -40 dbm.

* These three PC Boards are physically identical, but once the instrument has been calibrated they cannot be interchanged without requiring complete recalibration.



For $|A|$ large $\quad I_{in} = I_F = I_c \qquad (1)$

For $E_0 > .1$ V $\quad I_c = K' e^{\frac{q E_0}{kt}} \qquad (2)$

Then $I_{in} = K' e^{\frac{q E_0}{kt}} \qquad (3)$

And $E_0 = \frac{kt}{q} \text{ LOG } I_{in} - \frac{kt}{q} \text{ LOG } K' \qquad (4)$

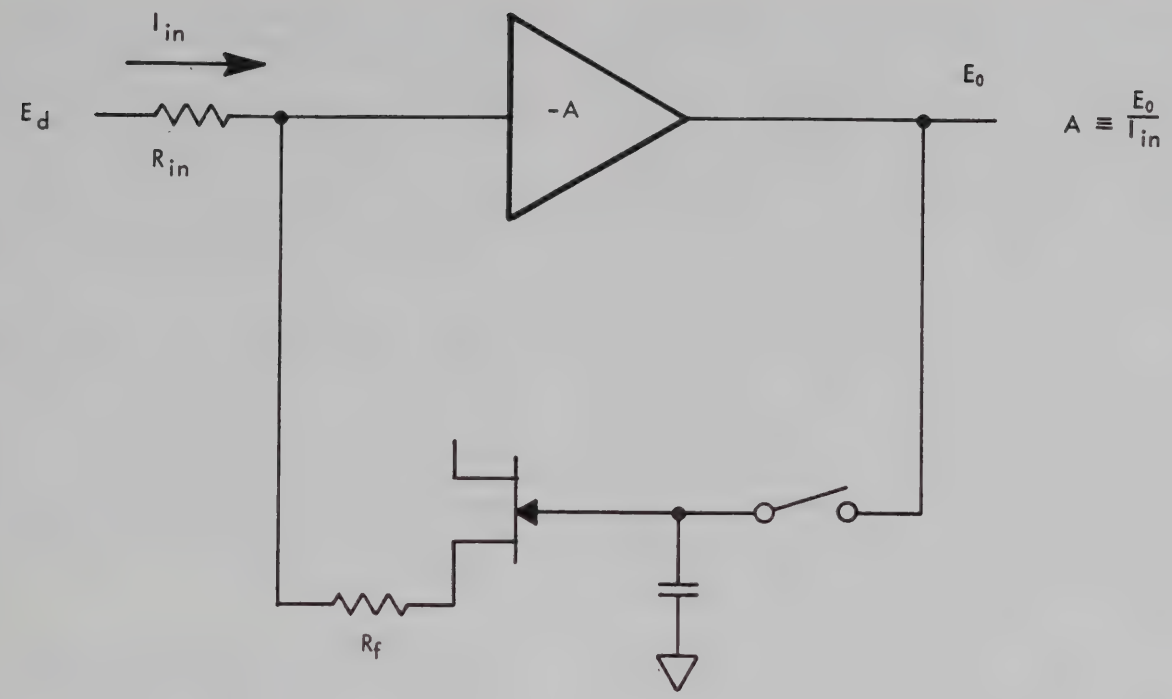
FIGURE 4-3. FUNCTIONAL DIAGRAM AND CHARACTERISTICS OF LOGARITHMIC AMPLIFIER CIRCUIT CONTAINED IN THE LOG CONVERTER AMPLIFIER (CHANNEL AMPLIFIER) A1/A2/A3

A simplified diagram of the logarithmic amplifier portion of the log converter amplifier is shown in Figure 4-3. The input circuit operates at ground level, allowing the feedback transistor to operate in the short-circuit collector mode which is required for true logarithmic response. The amplifier output voltage E_0 is of the proper polarity to forward-bias the base-emitter junction of the feedback transistor, another requirement for obtaining logarithmic feedback response. Under these conditions, the amplifier output voltage (v_{EB}) at point B can be shown to be related logarithmically to feedback current (i_C) by equation (2) in Figure 4-3, with high accuracy over a range well over six decades.

The short-circuit i_C vs v_{EB} transfer characteristic of the logging transistor is accurately logarithmic over this large dynamic range even though its other current-voltage characteristics are not. Among the circuit requirements for accurate logarithmic operation are: (1) v_{CB} must be held close to zero and not reverse-biased, so that the transistor operates in the short-circuit collector mode; (2) the input voltage drift must be kept very low; (3) the noise figure must be low; and (4) the operating range must be within the limits of v_{EB} = 0.1 V to i_C = 10 ma.

These requirements are met by use of the following techniques in the ALFRED logarithmic amplifier: (1) by use of high-gain differential stages in both the preamplifier and differential amplifier, and by using the logarithmic feedback to null out the detector current, v_{CB} is held closely at zero; (2), (3) the input stage is guarded, floated, and temperature-stabilized to keep noise and drift at an absolute minimum, and an automatic rebalancing circuit is provided to null out any drift effects after each presentation sweep; (4) the input range of less than 20 μv to more than 2 V, corresponding to incident power levels from -40 dbm to +20 dbm, provides output voltage and current within the prescribed limits.

The success of this circuit is due to the fact that v_{CB} of the logging transistor is essentially zero because of the high open loop gain of the amplifier and, thus, leakage currents in the collector-base region are negligible even for very low values of collector current. Note that the output sensitivity (in volts/db) of the logarithmic preamplifier, as given by equation (4) in Figure 4-3, is a direct function of temperature. Because of this, the logging transistor (A8Q2/Q4/Q6) is placed in a temperature regulated oven (Module A8). In order to minimize drift in the logarithmic amplifiers, the input differential pair of each channel amplifier (A8Q1/Q3/Q5) is also placed in the temperature regulated oven. Once the unit is up to operating temperature, drift should be no more than 3 db per hour at -40 dbm or 1 db per hour at -30 dbm.



$$\text{WITHOUT FEEDBACK } E_0 = -A\, I_{in} = \frac{-A\, E_d}{R_{in}} = E_0' \qquad (5)$$

$$\text{WITH FEEDBACK } E_0 = \frac{R_f\, E_d}{R_{in}} = E_0'' \qquad (6)$$

$$\frac{E_0''}{E_0'} = \frac{\frac{R_f\, E_d}{R_{in}}}{\frac{A\, E_d}{R_{in}}} = \frac{R_f}{A} < \frac{1}{10^5} \qquad (7)$$

FIGURE 4-4. FUNCTIONAL DIAGRAM AND CHARACTERISTICS OF AUTOMATIC REBALANCE CIRCUIT FOR LOGARITHMIC AMPLIFIER

To reduce the effects of drift to a negligible value, an automatic balancing circuit has been incorporated in the 7051. A simplified diagram of this circuit is shown in Figure 4-4. A high gain amplifier with feedback of the type illustrated is essentially self-balancing. That is, the feedback reduces the effects of drift considerably. Relay K1 closes only during the retrace period of each sweep, when no signal is present on the input of the logarithmic amplifier. The automatic balance circuit then acts to put feedback around the logarithmic amplifier during the retrace period. During the subsequent forward trace period when a signal is present in the input of the logarithmic amplifier, relay K1 is opened, and a memory capacitor, C9, in the automatic balance circuit maintains the drift correction signal on the FET transistor, Q8. Q8 draws negligible gate current, and thus maintains the drift correction signal on the amplifier, keeping it balanced even though the balancing feedback is not connected around it. Relay K1 is a reed relay, and its contacts are closed for approximately one millisecond during each retrace interval. The reed relay in each log amplifier channel is operated by a blanking pulse generated in the horizontal signal circuitry of the 7051 in Sweep Circuit A6. This pulse is triggered by the flyback of the horizontal sweep during retrace.

Requirements on the rf source so that the automatic balance may be used are that the source must be modulated completely off during retrace and that the retrace time be something more than 2 ms and less than 100 ms. The total time between sweeps should be greater than 5 ms. The automatic balance circuit will work for forward sweeps as slow as 1 second. All ALFRED Sweep Oscillators and Sweep Signal Generators meet these modulation and sweep requirements, as do many other swept rf sources.

To permit use with sources which do not meet the above characteristics, so that automatic balancing may not be used, a special operating mode is provided to permit quick, simple manual checking of drift, and each channel is easily balanced by means of a front panel control. By operating all low-level transistors in a regulated-temperature environment, drift is minimized to the point where manual rebalancing is required only a few times per hour. The tendency for input drift build-up is also minimized by the null-balancing negative feedback operation of the logarithmic amplifier.

The square-law compensation amplifier section of the log-converter amplifier, shown in Figure 4-2, consists of a differential amplifier input stage, an output amplifier, and a square-law compensation feedback network which is a diode shaper circuit. One input of the differential amplifier is driven by the output of the logarithmic amplifier, and the other input is driven by the compensation feedback network. The compensation network bleeds off feedback current over the intermediate and high-level amplifier output ranges to increase the gain at high levels to twice the low-level value, with a non-linear transition range.

At low levels within the square-law range of the detector, full negative feedback (i_{FB}) is applied through R_{FB} to R_B, to bias the differential amplifier for minimum gain. As the transition level is increased, an increasing amount of feedback current is shunted away from R_{FB}, to increase the gain in accordance with a non-linear curve that corrects exactly for the fixed non-linear shape of the transition region. The shunting effect increases to a fixed proportion of i_{FB} throughout the linear region, to provide twice the gain of the square-law region and thereby compensate for the reduced slope of the logarithmic amplifier output.

To compensate for the differences in power level at which the transition region occurs in various detectors, a biasing voltage is applied to the junction of R_{FB} and amplifier biasing resistor R_B through the panel CALIBRATION control. This adjustment of the return voltage of R_{FB} also adjusts the relative voltage level developed at point E by a particular feedback current through R_{FB}. The i_{FB}-shunting action of the diode-shaper compensation network is controlled by the voltage level applied to the biased diodes at point E. Hence, this method of adjusting the level developed at point E by any particular feedback current can adjust the point at which the non-linear transition range compensation begins, without altering the shape of the compensation curve. The range provided is sufficient to compensate for any detector, assuming that all detectors are square-law at -10 dbm, and linear at +10 dbm, with the transition range beginning anywhere inbetween.

4.2.1.1 Detailed Theory of Logarithmic Amplifier Circuit. In the logarithmic amplifier portion of the channel amplifier circuit, the circuit from A8Q1 through A1Q6 constitutes a dc-coupled, multi-stage differential amplifier which has feedback through A1R16 and logging transistor A8Q2. A8Q1 is a differential pair contained in a single can and located in the oven to maintain constant characteristics once the oven temperature is stabilized. The low-level balance of A8Q1 is adjusted by A1R35 and R20 in the emitter return circuit to -12.6 V. Use of a differential input stage provides common-mode rejection to cancel out any ripple effects from the instrument power supply or the test circuit, which is important in a sensitive amplifier such as this where the input sensitivity limit is ≈ 20 μv output from the crystal. The crystal detector input circuit is guarded, with the shell of the BNC INPUT jack connected to one differential input and the signal line connected to the other. A1R31 and A1R33 serve as input resistors for the signal and guard inputs at A1-E and A1-F, respectively. The INPUT connector shell is insulated from chassis ground to permit guarded, differential operation, so that grounding of the detector is accomplished through other ground connections within the test loop, i.e. the shell of the signal generator rf output connector. The common-mode rejection limit of the low-level input stage is a few hundred millivolts, so that the instrument cannot operate with the crystal detector "floating", but any ground return via the external test loop, such as through the center pin of the line cords of the sweeper and the 8000/7051, is satisfactory.

A1R32 and A1R34 provide a ground reference that keeps the signal input and ground return lines from floating when no crystal is connected. A1R31 in the signal input line constitutes a 10 K input load resistance for the crystal (since the A8Q1 bases operate at ≈ ground level). A1R33 provides a base input resistance for the A8Q1-A base to equal A1R31 in the B base circuit, thereby balancing the differential stage input impedances for stable operation. A1R9 provides power supply decoupling. A1R5, A1R37, and A1C2, A1C12, and A1C13 provide interference isolation for the input differential stage.

The R-C circuits between the collectors of each differential amplifier stage provide proper shaping of the gain vs signal frequency characteristic, to make the amplifier stable over its wide dynamic range with a large amount of non-linear negative feedback. A1R2, A1R4, A1R6, A1R8, A1R29, and A1R30 are the collector load resistors of the first three differential amplifier stages, from which the de-coupled output is obtained to drive the following stage.

The connection of A1Q5 and A1Q6 provides a single-ended output from the differential stages, at A1R15. With zero differential signal output from the A1Q3/A1Q4 stage, A1Q6 is biased to heavy conduction, so that its collector is close to ground level. An increasing input signal amplitude at the INPUT jack causes A8Q1B to conduct less heavily (ALFRED crystals provide negative polarity output), and this produces increased conduction in A1Q1, A1Q3, and A1Q5, and reduced conduction in A1Q2 and A1Q4, with the result that the forward bias on A1Q6 is gradually reduced, decreasing its conduction so that the output level increases toward the maximum.

The signal output of the logarithmic amplifier portion of the channel amplifier is obtained at pin A1-R, the emitter of the feedback logging transistor A8Q2. A1C7 and A1R16 provide feedback stabilization and restrict the output at A1-R to ≈ 7 mv/db within the square-law region. The 220 K resistance of A1R16 stabilizes the output-to-input feedback impedance over the 60 db performance range wherein the emitter-to-collector impedance of the logging transistor undergoes drastic change. The collector current of the transistor is proportional to the logarithm of the emitter-base voltage. The positive current from the A8Q2 feedback transistor thus cancels the negative signal input current at the base of A8Q1-B when the output voltage represents the logarithm of the input signal. The feedback thus causes the amplifier output to follow the input signal logarithmically. Capacitor A1C8 across the feedback resistor compensates for any parasitic capacitances to ground in the vicinity of pin A1-R.

At an input signal level corresponding to -40 dbm, the emitter-to-base resistance of the logging transistor is about 25 megohms, while at an input signal level corresponding to +20 dbm, the emitter-to-collector resistance drops to about 25 ohms. With the 220 K series feedback resistor, the variation is from 25

megohms to 220 K ohms, about a 100:1 range. The loop gain, therefore, also changes by about a 100:1 ratio, being greater at low levels as required to obtain logarithmic response. Since the gain-bandwidth product of the amplifier is essentially constant, the bandwidth is reduced at low levels and this helps minimize the effects of noise without sacrificing response speed at higher levels. The amplifier bandwidth at signal levels corresponding to -40 dbm input is several KHz, while above -20 dbm it is 1 MHz or greater. A1C10, connected across the logging transistor, provides a high frequency feedback bypass to avoid attenuation or phase shift of high frequency feedback components due to the collector capacitance of A8Q2 or the coaxial feedback connection line. Thus, the overall logarithmic amplifier circuit is similar to an operational amplifier in which A1R31 is the input summing resistor and A1R16 plus the transfer characteristic of A8Q2 constitutes the feedback resistance. Proper logarithmic response of A8Q2 requires that the collector of A8Q2 be held close to ground, and this is achieved by its connection to the feedback summing junction which is maintained at near-zero level by the differential amplifier mode of operation. While the differential amplifier operation rejects common-mode signals in the amplifier output, excessive common mode signals (which elevate both base leads of A8Q1), will cause the collector of the logging transistor to be raised far enough above ground level that the logarithmic response may be impaired.

The amplifier output of ≈ 7 mv/db at low levels drops to about 3.5 mv/db at high levels because of the crystal response transition from square-law to linear response. The remainder of the channel amplifier, the square-law compensation amplifier, provides a variable-gain characteristic varying from about 14:1 at low levels to 28:1 at high levels, with a gain variation shape that matches the logarithm of the standard crystal response curve through the crystal transition region. Thus, the compensation amplifier maintains a fixed 1 V/db output over the full 60 db dynamic operating range.

4.2.1.2 Detailed Theory of Square-Law Compensation Amplifier Circuit. The compensation amplifier is a dc amplifier consisting of two differential stages followed by a single-ended amplifier stage. A1Q9A receives the logarithmic amplifier output while the variable negative feedback which controls the amplifier gain is applied to A1Q9B. The output from the first differential pair is applied to A1Q10 in the second differential pair, while A1Q12 is driven by a voltage divider between + 12.6 V and ground. The output of the second differential pair is amplified by a single-ended stage, A1Q11.

A1R45 isolates the feedback diode-shaping network from the signal output line, and A1R52 serves as the feedback resistor. The diode shaping network bleeds off current from A1R52 at intermediate and high-level amplifier output ranges to increase the gain by a factor of two. Diodes A1CR4 through A1CR7, which shunt current away from A1R52, are returned to different bias voltages provided by separate pairs of voltage-divider resistors, connected between +12.6 V and -12.6 V.

The R-C networks consisting of A1C14/A1R39 and A1C15/A1R42, and A1C16 provide feedback compensation to make the amplifier stable. Diodes CR2 and CR3 provide temperature compensation for the diodes in the shaping network. The CHN +10 CAL Control adds an adjustable current to the feedback at the A1Q9B base, to adjust the signal amplitude at which the feedback becomes effective in altering the gain, without affecting the shape of the gain characteristic which is controlled by the current increment supplied by the diode shaper board.

4.2.1.3 Detailed Theory of Automatic Rebalance Circuit. The automatic balance circuit utilizes the "rf off" retrace characteristic of the typical sweeper to perform a balance operation on the amplifier. During retrace, with no rf signal input to the crystal detector, the video input and output of the logarithmic amplifier should be exactly zero. In order to correct for any non-zero amplifier output, a 1-megohm feedback resistor (A1R24) is temporarily connected between the amplifier output and input to provide negative feedback that will drive the output to essentially zero in the absence of an input signal.

A1R24 is not connected directly to the logarithmic amplifier output at pin A1-R, but instead is driven by an output isolation and switching circuit which prevents the balancing feedback loop from loading the amplifier and which connects the amplifier output to the circuit only during the automatic balancing interval.

Amplifier A1Q7 is an emitter follower which provides unity gain and isolates the feedback circuit from the amplifier output. A1Q7 taps off the full voltage developed at the A1Q6 collector before attenuation in the feedback resistor A1R16. Diode A1CR1 compensates the emitter-base temperature characteristic of A1Q7. Relay A1K1 is energized during the retrace interval when operation is in the automatic balance mode, and applies the isolated output signal to FET transistor A1Q8. Capacitor A1C9 stores the signal to provide a "memory" function during the subsequent measurement interval when K1 disconnects A1Q8 from the amplifier output. A1C9 is charged through a low impedance (A1R19) driven by the low impedance output of Q7, to provide a short time constant because only about a millisecond is available for changing A1C9 to the correct level in fast sweep operation.

The rebalance signal supplied by the sweep circuit energizes relay A1K1 during the first 1.5 ms of each sweep retrace interval in the automatic balance mode, regardless of sweep speed. This short duration is compatible with the fastest retrace performance of sweepers such as the ALFRED Model 630/640/650, which have a retrace interval slightly greater than 2 ms at the fastest sweep speeds. The 1.5 ms charging interval, combined with the limited amplifier bandwidth at the low level used for rebalancing, allows storage capacitor A1C9 to be charged to the level that produces output-zeroing feedback to the input; and then disconnects the capacitor before the rf is again applied, so that the proper feedback signal is maintained throughout the next measurement interval. The output of the amplifier retains a slight residual positive offset as required to maintain the feedback signal which reduces drift effects to that level, but as calculated in Figure 4-4, this residual drift is less than 1×10^{-5} of the drift that would be present without automatic balancing.

A FET transistor is chosen for the A1Q8 stage because of its low leakage currents and low base currents, to preserve the charge storing capability of the memory capacitor, avoiding drift during the forward trace. This memory capability, and the excellent stability of the amplifier, permit operation in the automatic balancing mode with sweep times as slow as one second. The FET transistor operates as a source follower amplifier (similar to an emitter follower) and the signal across its output resistor, A1R26, is connected directly to the balancing feedback resistor A1R24 by a direct external connection between pins A1-S and A1-V which is supplied by the DISPLAY MODE selector switch.

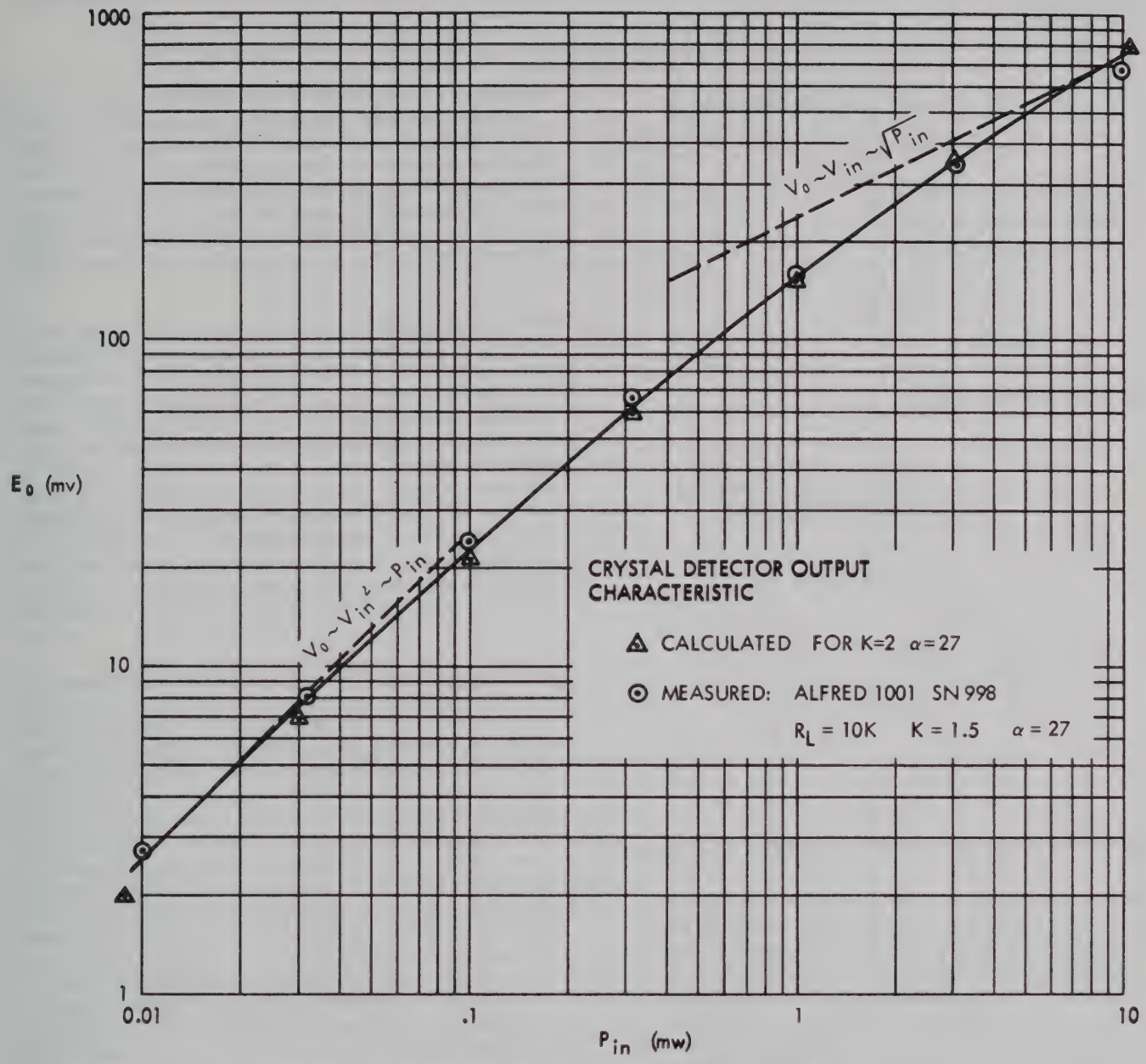


FIGURE 4-5. REPEATABILITY OF CRYSTAL DETECTOR CHARACTERISTICS

4.2.1.4 Detailed Theory of Manual Balance Adjustment Circuit. For slow sweeps, where the sweep time is longer than 1 second, for manually triggered sweeps (where the sweeper generates a single-frequency signal at one end of the spectrum until triggered), for sweepers in which the rf output is not turned completely off (some sweepers reduce the signal as little as 30 db during retrace), and for single-frequency measurement, a manual balancing mode is provided.

With the BALANCE switch S3 in MANUAL, pins S and V are grounded in the RATIO, LOG, and CAL modes, to provide a ground-level reference to the amplifier input. Pin U is open-circuited by S3 to keep relay A1K1 de-energized so the automatic balance circuit is inactive. In the BAL mode, the external connection is not made between pins A1-S and A1-V, and neither pin is grounded. Pin U is grounded by S3 to energize relay A1K1. Then 22-megohm resistor A1R23 is added into the signal feedback circuit between the output of A1Q8 and the input of A8Q1. This effectively increases the gain of the amplifier by 22:1 so that a 10 μv input drift offset would appear as a 22 mv offset at the amplifier output. Relay K1 is continuously energized in the manual balancing mode so that any offset voltage on the amplifier input is amplified and coupled through to pin A1-V. The A1-V output is connected directly to the chopping circuit, bypassing the summing amplifier, to provide maximum display sensitivity. The chopping circuit amplifier produces zero output with zero input.

The Balance controls (A1R35 and R20) can then be used to set the amplifier input to an exact balanced condition, as indicated when the CRT trace is centered, indicating absence of any amplified offset signal at the output of the logarithmic amplifier circuit. The manual balance procedure permits balancing with the crystal connected to the point of measurement so that the same thermal environment experienced in the test loop will exist under balancing conditions. Otherwise, thermal emf's could produce error or offset in the balance adjustment.

4.2.2 CRYSTAL DETECTOR COMPENSATION CHARACTERISTICS. Until now, crystal detectors were considered to have usable outputs only in the square law region, that is, where the DC output voltage of the detector was directly proportional to its rf input power. Utilizing only the square law region of the crystal limits one to making measurements in the region where the rf input to the crystal is below -10 dbm and above noise. This corresponds to a dynamic range of some 30 db.

A detailed study of a wide variety of crystal detectors, including both laboratory measurements and theoretical calculations, showed that all commonly-used crystals have a uniform response curve shape through the square-law, transition, and linear regions, as shown in Figure 4-5. This condition holds within a small fraction of a db for crystals which have a video resistance at least twice that of the detector load. Only the actual power level at which transition occurs differs between crystals. By providing a constant-shaped compensation curve for non-square-law performance, with a simple adjustment of the level at which the transition range compensation begins, as described in Paragraph 4.2.1, the overall response can be quickly adjusted for near-perfect compensation of any commonly used crystal detector.

The equations which define ideal crystal performance characteristics, without considering square-law limitations, are given in Part A of Figure 4-6. The point contact crystal rectifiers used in ALFRED ELECTRONICS crystal detectors, such as the superior Model 1001, have an α approximately equal to 27. R_{int}, the video resistance, normally varies between 10 K and 20 K, and is limited to less than 20 K in current production of the Model 1001. Below -10 dbm the equation shown in Part A of Figure 4-6 reduces to that shown in Part B, which is the square-law approximation. As might be expected at high levels (above +10 dbm), the crystal detector merely acts as a peak detector with the DC output voltage being directly proportional to the rf input voltage. In the transition region between the square law and linear law regions, the crystal characteristic is, of course, neither square law nor linear; but it is, however, predictable. An interpretation of the mathematics shows that for K fixed, all crystals have identically shaped output characteristics. This is substantiated by the plot of Figure 4-5, which shows the calculated and measured values of a typical crystal characteristic in the transition region. As can be seen from the plot, measured values agree quite well with calculated points.

A. IDEAL CRYSTAL DETECTOR

$$(1+K\alpha E_{dc})\, e^{\alpha E_{dc}} = I_0\,(\alpha E)$$

E_{dc} = DETECTOR OUTPUT

E = PEAK RF INPUT VOLTAGE ($E_{in} = E \cos \omega t$)

$K = \dfrac{R_{int}}{R_L}$

$\alpha \approx \dfrac{q}{kt} \approx 20$ to 35

I_0 - MODIFIED BESSEL FUNCTION

B. CRYSTAL CHARACTERISTIC SQUARE LAW APPROXIMATION

$$E_{dc} = \frac{\alpha E^2}{4(1+K)} \qquad \text{for } P_{in} < -10 \text{ dbm}$$

E_{dc} = DETECTOR OUTPUT

E = PEAK RF INPUT VOLTAGE ($E_{in} = E \cos \omega t$)

$K = \dfrac{R_{int}}{R_L}$

$\alpha \approx \dfrac{q}{kt} \approx 20$ to 35

FIGURE 4-6. CRYSTAL DETECTOR PERFORMANCE EQUATIONS

Only the actual input power level at which departure from square law occurs varies from crystal to crystal. Variations in K cause the shape of the curve to change slightly but as long as $K < 2$, this effect is slight and compensation accurate to within a fraction of a db is possible. Since R_L, the log converter amplifier input impedance, is 10 K, this condition will be met as long as video impedance is kept under 20 K ohms. This being the case, the log converter amplifier is designed so that it will compensate accurately for the crystal when it is operating above the square law region, with only a single calibration adjustment required.

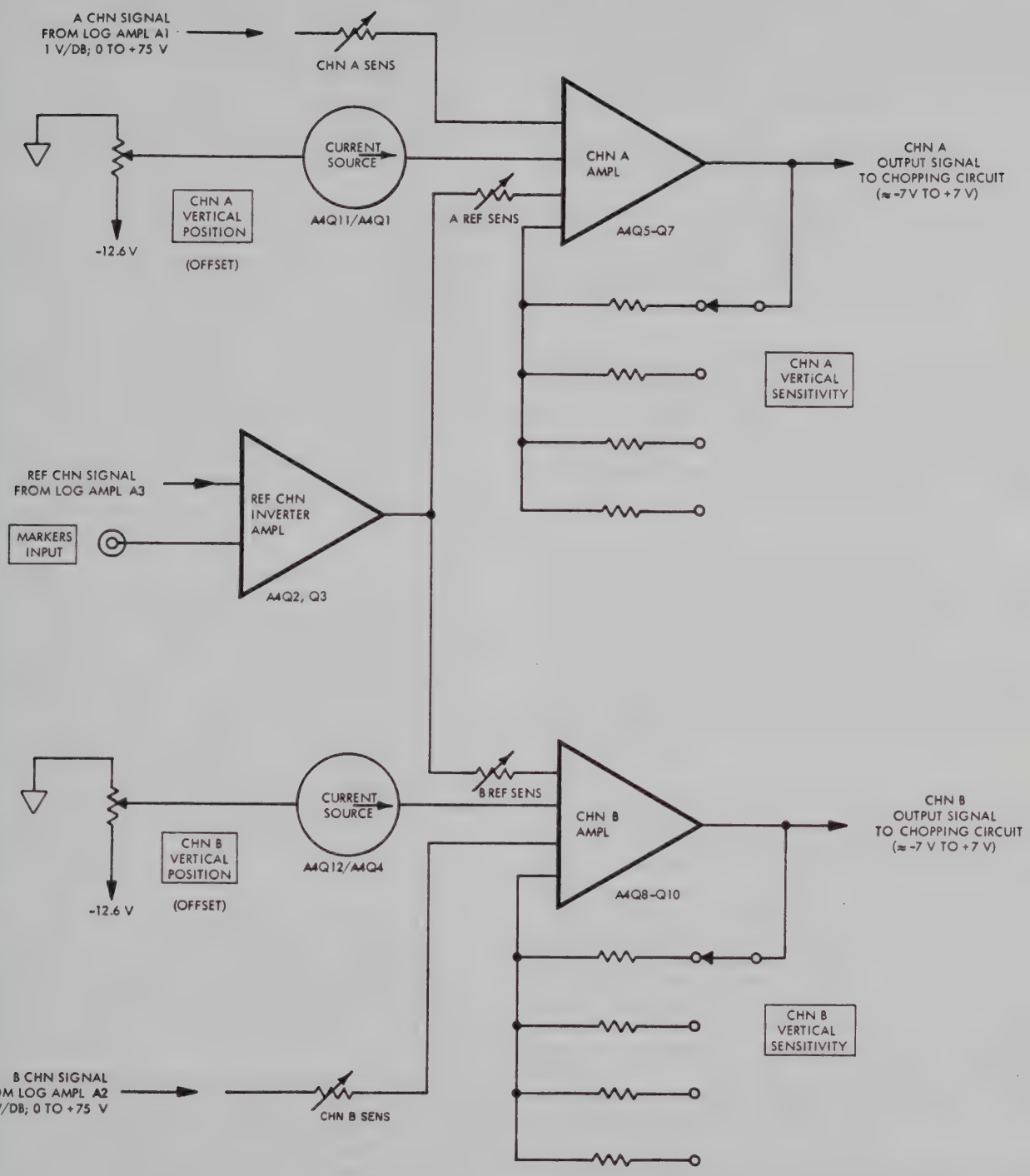


FIGURE 4-7. BLOCK DIAGRAM OF SUMMING AMPLIFIER (A4)

4.2.3 SUMMING AMPLIFIER. (See Figure 4-7 and Schematic 900825C.) The A and B Channel log converter outputs are applied to the corresponding operational summing amplifiers (A4Q5 - A4Q7 and A4Q8 - A4Q10), where they represent the measured level for absolute measurements, or the numerator of the ratio fraction for ratio measurements.

The reference channel log-converter amplifier output is inhibited for absolute measurements. For ratio measurements, it is applied to both summing amplifiers, after a polarity inversion (in A4Q2 and A4Q3), to serve as the denominator of both ratios. An input for video marker pulses, such as supplied by the ALFRED 650 Series Sweep Oscillators, is also applied to the summing amplifiers and permits a handy frequency calibration of the CRT presentation.

The use of analog computation techniques, operating on voltages that logarithmically represent the parameters being mea-

sured, permits development of a ratio readout by simple summation of voltages of opposite polarity. These techniques also permit simple, yet accurate adjustment of measurement sensitivity and calibration offset with precision dc circuits rather than more expensive, limited-range microwave components. Precision multi-turn potentiometers and dc voltage supplies within the measurement system can thus accomplish the same function over the full measurement range that would otherwise require considerable precision hardware in the external test circuit for each different frequency band.

An adjustable input of either polarity can be applied independently to each summing amplifier by means of a panel VERTICAL POSITION control. This offset input can balance out the net signal difference at the summing junction corresponding to any value from 60 db gain to 60 db loss. Thus, any level of operation can be offset for high-sensitivity examination on the CRT; and alternately, any absolute level developed by a particular detector being driven by the internal rf calibrator can be matched for calibration of the CRT at any desired power level. Each offset signal output is applied to the corresponding summing amplifier through a current generator isolation stage (A4Q11/A4Q1 or A4Q12/A4Q4) to avoid loading the offset potentiometer. The amplification thereby provided also permits the offset potentiometers (R8 and R9) to be driven from the well regulated -12.6 V supply.

Each offset control also operates a mechanical 3-digit counter mechanism which indicates db offset directly in 0.1-db increments up to ± 60 db, and identifies the offset as either gain or loss. By turning a concentric knob, the control potentiometer is disengaged from the counter and knob drive. This allows any desired reference counter setting (unity ratio or 0 db for example) to be made after the offset control potentiometer has been set to compensate for insertion loss of couplers, etc. in the external test circuit under calibration conditions. With the counter set to read 0 db under unity-ratio calibration conditions, the offset control can be used to return any portion of the performance trace to exactly the calibration position on the graticule, and the gain or loss ratio can be read directly in db from the counter.

The presentation sensitivity is adjusted by adjusting the gain of each summing amplifier over a 20:1 range in db using separate panel SENSITIVITY controls for each channel. This provides a CRT presentation sensitivity range from 0.5 db/cm to 10 db/cm, and a recorder output sensitivity of 0.5 db/division to 10 db/division.

4.2.3.1 Detailed Theory of Summing Amplifier. The design input sensitivity of each summing junction is about 13 μa/db. The summing junction of the A Channel summing amplifier is the base of A4Q5, and the summing junction of the B Channel summing amplifier is the base of A4Q8. The output sensitivity of each summing amplifier is independently controlled by adjusting the feedback current to the summing junction by means of the feedback resistor selected by each VERTICAL SENSITIVITY control.

The net signal developed at the summing junction to drive the amplifier is the sum of the signal currents from the Signal Channel (A or B) input, the Reference Channel input, and the calibrated Offset current. In response to any net input current level, the summing amplifier developes an output voltage such that the negative feedback current developed through the feedback resistor exactly cancels the net positive input current. The operation of each source of current at the input summing junction of each summing amplifier is discussed in detail below.

4.2.3.2 Development of A or B Channel Signal Input Current. The Channel A and Channel B signal input current is developed from the ≈ 1 V/db signal supplied to A4-B and A4-Y from Channel Amplifiers A1 and A2, respectively. This voltage, applied through A4R2, A4R3 or A4R12, A4R13 (with the Sens. resistor adjusted near its center position) produces an increasing positive current of ≈ 13 μa/db at the base of A4Q5 or A4Q8.

4.2.3.3 Development of Ref Channel Signal Input Current. The Ref Channel input voltage of ≈ +1 V/db is applied to A4-E, and its slope is inverted by unity-gain amplifier A4Q2/A4Q3 to develop a voltage that is still positive but has a slope of -1 V/db at the junction of A4R25 and A4R27. The two-stage amplifier is a feedback-controlled operational amplifier with a signal input resistor (A4R7) of 80.6 K and a feedback resistor (A4R6) of identical value to give unity gain with inversion.

With 0 V input at the base of A4Q2, that transistor is biased to very light conduction, so that the drop across A4R10 is sufficient only to bias A4Q3 to light conduction. The current drawn through load resistor A4R16 by A4Q3 drops the inverter amplifier output voltage (at the A4Q3 collector) to ≈ +60 to +70 V. With maximum input (≈ +70 V) at A4-E, A4Q2, and A4Q3 are driven to heavy conduction, and the amplifier output drops to ≈ 0 V.

Thus, the inversion amplifier supplies an output which decreases at the rate of 1 V/db from ≈ +70 V when there is no signal input to the Reference Channel to ≈ 0 V when there is maximum Reference Channel signal input. This voltage, applied through A4R27, A4R17, A4R25, A4R26, produces a decreasing positive reference signal input current of ≈ 13 μa/db at the two summing junctions. This current varies from ≈ 750 μa corresponding to zero reference signal to ≈ 0 μa corresponding to maximum reference signal.

NOTE: The reference signal current output thus has the same slope as if it ranged from 0 μa to -750 μa, as required to provide the logarithmic subtraction of the ratio denominator (Ref Channel) from the numerator (A or B Channel). The reference signal current can be interpreted as consisting of a variable 0 μa to -750 μa current generator summed with a fixed +750 μa current generator. In operation, the variable 0 to -750 μa current generator can perform its proper subtractive function because the fixed +750 μa current is cancelled by the -750 μa current generated by the Offset control current source (discussed below) at the mid-range zero offset point. This arrangement provides the simplest and most reliable means of allowing the Offset control to provide both gain and loss offset, having the effect of both positive and negative polarity signal currents, while requiring only a single-polarity source.

4.2.3.4 Development of VERTICAL POSITION Offset Input Current. The Offset control current sources A4Q1 and A4Q4 generate a negative current with a sensitivity of ≈ -13 μa/db, corresponding to the Offset control setting over a dynamic range of > 120 db (which provides offset of 60 db gain, through 0 to 60 db loss). Thus, with either Offset control fully CW, corresponding to maximum LOSS DB offset, the Offset control potentiometer R8 or R9 applies ≈ -12.6 V to the base of the current source driver transistor A4Q11 or A4Q12. The driver transistor conducts heavily and the drop across load resistor A4R33 or A4R34 applies ≈ -12.6 V to the base of the current source transistor (A4Q1 or A4Q4), to cut it off so that no negative current is supplied to the summing junction.

The absence of negative offset current means that no positive current is drawn from the junction, so that the full signal current from the Ref and A Channels is available to drive the summing amplifier. Thus, if a 60 db loss ratio exists (i.e. zero input voltage and signal current on the Signal Channel and maximum input voltage with zero signal current on the Reference Channel) the summing junction net of zero current will center the display on the CRT.

With the Offset control set at mid-position, corresponding to 0 DB GAIN or LOSS offset, the Offset control pot supplies ≈ -6.3 V to the base of the current source driver transistor. The driver output tracks the input, applying ≈ -6.3 V to the base of the current source transistor. This biases the current source transistor to moderate conduction so that it generates a negative current of ≈ -750 μa. This negative current has the effect of drawing the same amount of current from the summing junction, thereby bleeding off the exact signal current generated by the Reference Channel when zero reference signal exists. Thus, if unity ratio exists (i.e. zero input voltage and signal current on the Signal Channel and zero input voltage with maximum current on the Reference Channel, or any identical-level combination, which also produces ≈ +750 μa total signal current since the Reference Channel current decreases at the same rate the Signal Channel current increases), the +750 μa total signal current and the -750 μa Offset current will cancel, and the summing junction net of zero current will center the display on the CRT.

With the Offset control fully CCW, corresponding to maximum GAIN DB offset, the Offset control pot supplies ≈ 0 V to the base of the current source driver transistor. This further reduces the driver transistor conduction, so that the output tracks the input. The ≈ 0 V bias thereby applied to the base of the current source transistor biases it to heavy conduction so that it generates a negative current of ≈ -1.5 ma. This draws off 1500 μa of current from the summing junction, bleeding off both the maximum signal current generated by the Reference Channel and the Signal Channel. Thus, a zero current net at the summing junction is obtained when a 60 db gain ratio exists (corresponding to maximum input voltage and signal current on the Signal Channel and minimum input voltage with maximum signal current on the Reference Channel), and the display on the CRT is centered.

Any combination of signals which does not exactly cancel at the summing junction will drive the display above or below the CRT centerline by an amount related to the non-zero offset. Thus, if a gain ratio is measured which is larger than the GAIN DB Offset applied, or if a loss ratio is measured which is smaller than the LOSS DB Offset applied, there will be a net positive current at the summing junction to drive the trace upwards. If a gain ratio is measured which is smaller than the GAIN DB Offset applied, or if a loss ratio is measured which is larger than the LOSS DB Offset applied, there will be a net negative current at the summing junction to drive the trace downwards.

4.2.3.5 Calibration of Input Signal Sources. The VERTICAL POSITION Offset current generators are used as the calibration standards for the Summing Amplifier. The Channel A, Channel B, A Ref, and B Ref Sensitivity potentiometers are all set to provide identical μa/db response to that of the Offset current generator. The calibration PRESET arrangement on the Offset controls allows them to be zero-set at a level which corresponds to the zero-voltage signal current in the Reference Channel.

4.2.3.6 Disabling the Reference Channel for LOG and CAL Modes. When the instrument is operated in any LOG mode, or in the A CHN or B CHN CAL modes, the signal level applied on either Signal Channel input is to be amplified alone, without ratio conversion. To achieve this, a +12.6 V signal is applied to A4-F by the DISPLAY Mode Selector switch. The +12.6 V input, applied to the base of A4Q2 through A4R5, drives the inversion amplifier to heavy conduction so that it supplies zero output voltage and zero current to the summing junction. The summing junction then is controlled by the net current difference between the Signal Channel input current and the Offset current. VERTICAL POSITION Offset digital counters can be zero-set to indicate 0 dbm when the Offset control is set to null out the signal current produced at the summing junction by a 0 dbm calibration signal.

Since the A and B Channel signal currents are zero when no signal is applied, no similar arrangement is required to disable those signals in the REF CHN CAL Mode when the signal is applied only to the Reference Channel.

4.2.3.7 Summing Amplifier Operation. Each summing amplifier is a high-gain operational amplifier consisting of a differential input stage and a single-ended output stage. A4Q5, A4Q6, and A4Q7 constitute the A Channel summing amplifier, and A4Q8, A4Q9, and A4Q10 constitute the B Channel summing amplifier. Each amplifier provides an output inversion, so that a positive current input at the summing junction produces a negative output signal. For example, a positive current applied to the base of A4Q5 increases its conduction and the differential amplifier response reduces the current through A4Q6.

The reduced current through A4Q6 increases the positive bias on the base of A4Q7, reducing its conduction and decreasing the current through output resistor A4R21. This reduces the output voltage. Since A4R21 is returned to -12.6 V while the emitter of A4Q7 is returned to +12.6 V through A4R15, the output voltage can be of either polarity.

The output sensitivity referred to the CRT (controlled by the subsequent amplification stages in the Chopping Circuit A5) is ≈ 1.3 V/cm, so that for on-scale presentations, the summing amplifier output voltage may range from -6.5 V to +6.5 V. For zero net summing junction current, A4Q7 is driven to moderate conduction to provide 0 V output. The relation of output voltage to summing junction input current for non-zero signals is controlled by the feedback resistor selected by the VERTICAL SENSITIVITY switch. The amplifier responds to any input current level by increasing the output voltage of opposite polarity to the point where the feedback current equals the summing junction input current. Thus, since the input sensitivity of the summing junction at the input to the summing amplifier is ≈ 13 μa/db, the feedback resistors have a value that relates this to the output sensitivity of 1.3 V/cm. For example, the 100 K resistor used for the 1.0 DB/CM VERTICAL SENSITIVITY setting derives a 13 μa feedback current from a 1.3 V signal, as required to cancel a 13 μa summing junction net input signal corresponding to a 1 db ratio readout. Capacitors A4C1, A4C2, A4C4 and A4C5 are supply decoupling capacitors. The R-C networks A4C3/A4R22 and A4C6/A4R32 provide response stability in the amplifier.

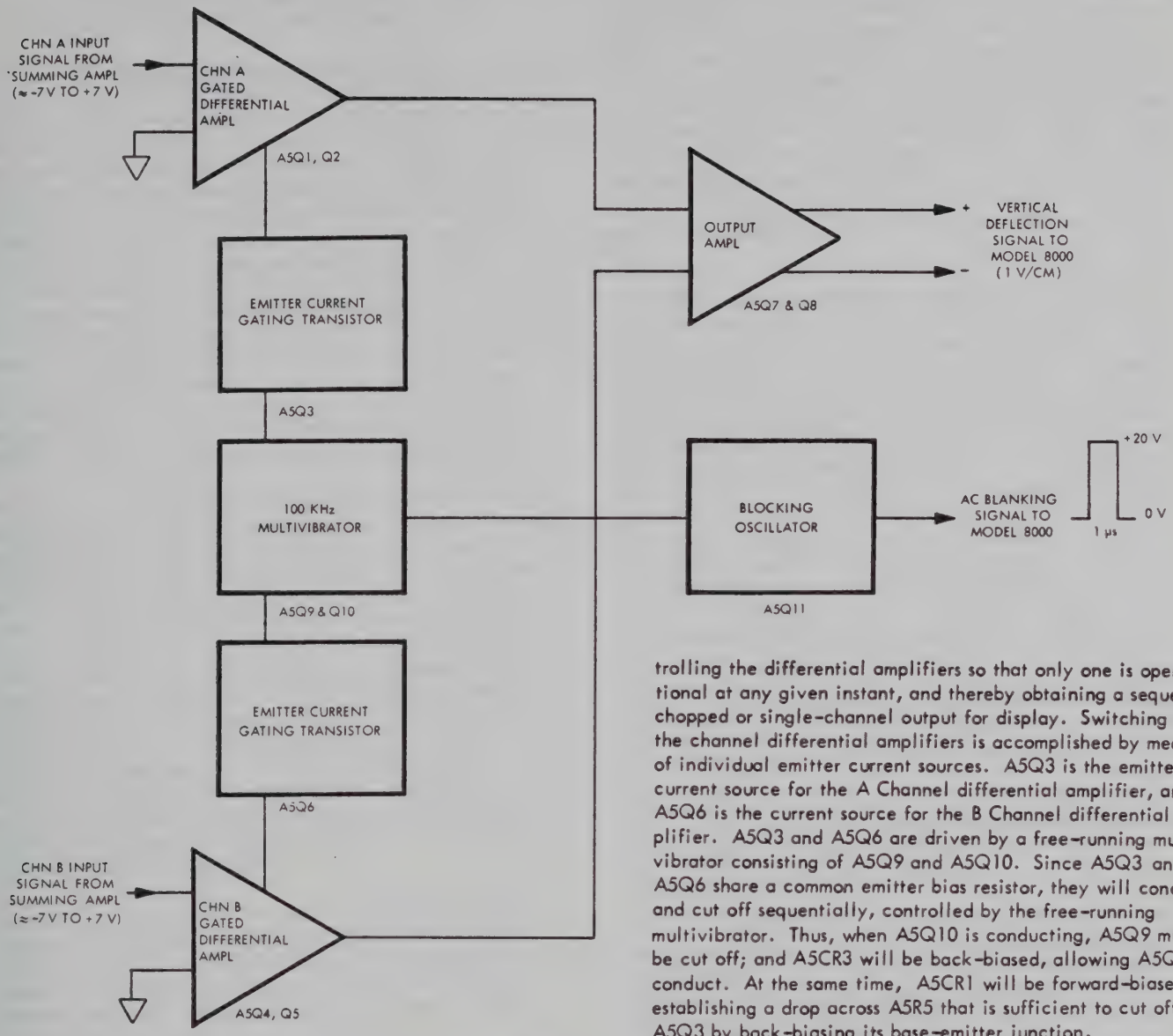


FIGURE 4-8. BLOCK DIAGRAM OF CHOPPING CIRCUIT (DISPLAY SWITCH) A5

4.2.4 CHOPPING CIRCUIT (DISPLAY SWITCH). (See Figure 4-8 and Schematic 900826C.) A display switch consisting of a 100 KHz solid-state chopper (A5Q1 - A5Q10) is used to multiplex the Channel A and Channel B outputs to generate the vertical signal for the Model 8000 Oscilloscope. The chopper circuit also generates a 1-µs "ac blanking" pulse during each switching interval (with A5Q11), to blank the trace as it switches between segments of the chopped dual-channel presentation. The display switch can be set in either position to allow single-channel presentation if desired. This is useful for driving an external recorder, allowing readout of each channel individually on successive slow sweeps.

In the solid-state chopper circuit, A5Q1 and A5Q2 constitute a differential amplifier for the Channel A signal, and A5Q4 and A5Q5 constitute a differential amplifier for the Channel B signal. The corresponding stages of each differential amplifier share a common collector load resistor, which permits controlling the differential amplifiers so that only one is operational at any given instant, and thereby obtaining a sequential chopped or single-channel output for display. Switching of the channel differential amplifiers is accomplished by means of individual emitter current sources. A5Q3 is the emitter current source for the A Channel differential amplifier, and A5Q6 is the current source for the B Channel differential amplifier. A5Q3 and A5Q6 are driven by a free-running multivibrator consisting of A5Q9 and A5Q10. Since A5Q3 and A5Q6 share a common emitter bias resistor, they will conduct and cut off sequentially, controlled by the free-running multivibrator. Thus, when A5Q10 is conducting, A5Q9 must be cut off; and A5CR3 will be back-biased, allowing A5Q6 to conduct. At the same time, A5CR1 will be forward-biased, establishing a drop across A5R5 that is sufficient to cut off A5Q3 by back-biasing its base-emitter junction.

With A5Q3 cut off, no current is available for the Channel A differential amplifier, and it is effectively switched "off" while the Channel B differential amplifier is switched "on". The opposite is true when multivibrator stage A5Q10 is conducting and A5Q9 is non-conducting. When operating in the chopped presentation mode, the free-running multivibrator is allowed to oscillate and the display alternately switches between the A and B Channels. When a single-channel presentation is selected, a ground-level reference signal is supplied to the appropriate multivibrator base by the DISPLAY Mode Selector switch (via J5-E and J5-H) to hold the multivibrator in the proper state to disable the undesired channel.

Transistors A5Q7 and A5Q8 are emitter follower output amplifiers used to isolate the differential amplifiers in the chopping circuit from the vertical amplifier in the Model 8000. Transistor A5Q11 and transformer A5T1 constitute a blocking oscillator which generates the "ac blanking" pulse to blank the Model 8000 CRT display each time the chopper multivibrator switches. The positive-going pulse from each side of the multivibrator is coupled to the base of A5Q11 through A5CR2 and A5CR3. The blocking oscillator output, at J5-T, is a 20 V, 1 µs pulse.

4.2.4.1 Detailed Theory of Chopping Circuit. The individual circuits of Chopper PC Board A5 are discussed in detail below Circuit waveforms are shown in Figure 5-6 (page 5-19).

4.2.4.2 Multivibrator Circuit and Amplifier Gating Transistors. In all dual-channel presentation modes, the "reference level" inputs at A5-H and A5-E are open-circuited, so that the 100 KHz multivibrator A5Q9 and A5Q10 is free-running. The free-running operation is conventional. Each multivibrator transistor has a split load resistor (A5R27/A5R28 or A5R31/A5R33), with the cross-coupling capacitor (A5C8 or A5C9) connected from the load resistor split point to the base of the opposite stage. When one transistor begins conduction, the positive pulse applied to its output coupling capacitor is coupled to the base of the other transistor to reinforce cut-off. That base connection of the capacitor then begins charging toward -12.6 V, and when it becomes more negative than -0.6 V, the opposite transistor is turned on and the previously conducting transistor is cut off by the same action. The R-C time constants of the charging circuits (A5C8/A5R29 and A5C9/A5R30) are such that the multivibrator free-runs at 100 KHz.

The multivibrator output is obtained from the A5Q9 and A5Q10 collectors. It controls the differential amplifier emitter current source stages A5Q3 and A5Q6. Operation is as follows: When A5Q9 is conducting, its collector is raised almost to ground level, more positive than the junction of A5R5 and A5R6, which is part of a voltage divider (with A5R7) between ground and -12.6 V. Thus, A5CR1 is back-biased; and similarly, A5CR3 is forward-biased since the A5Q10 collector is dropped to ≈ -12.6 V during cut-off. A5CR1 thus isolates the base-bias network of A5Q3, while A5CR3 couples the junction of A5R21 and A5R22 to ≈ -12.6 V. The result is that A5Q3 is biased to conduction by its base bias network, while A5Q6 is cut off. Only the Channel A differential amplifier (A5Q1/A5Q2) then receives emitter current, so that it controls the output amplifiers A5Q7 and A5Q8, and the Channel B differential amplifier (A5Q4 and A5Q5) is inoperative.

Conversely, when A5Q10 is conducting, the biasing of the cathodes of A5CR1 and A5CR3 is reversed, so that A5Q6 is biased to conduction while A5Q3 is cut off. Then only the Channel B differential amplifier receives emitter current and it controls the output amplifiers while the Channel A differential amplifier is inoperative.

When a single-channel presentation mode using only the B Channel is selected, the DISPLAY Mode Selector switch applies a ground level signal to A5-H, thereby holding A5Q9 cut off, while A5-E remains open-circuited. This allows A5Q10 to conduct continuously, because cut-off triggering action that would normally take place when A5C8 charged to the turn-on level of A5Q9 is inhibited. Thus, A5CR3 is continuously back-biased, allowing A5Q6 to conduct to operate only the B Channel differential amplifier for a continuous B Channel display.

Conversely, when a single-channel presentation mode using only the A Channel is selected, the DISPLAY Mode Selector switch applies a ground-level signal to A5-E, thereby holding A5Q10 cut off, while A5-H remains open-circuited. This allows A5Q9 to conduct continuously, to operate only the A Channel differential amplifier for a continuous A Channel display.

4.2.4.3 Gated Differential Amplifiers and Output Amplifier. Since the A and B Channel differential amplifier circuits are identical, only the A Channel amplifier circuit will be described in detail. The single-ended input from the A Channel summing amplifier in A4 (or directly from the logarithmic amplifier being manually balanced in the BAL operating mode) is applied to A5-A where it drives the base of A5Q1. The base of the other transistor of the differential pair, A5Q2, is tied to ground. Thus, since both the summing amplifier output and the logarithmic amplifier drift can be of either polarity, the relative conduction of each half of the differential pair will be determined by the polarity and magnitude of the input signal.

The current through load resistors A5R14 and A5R15 will be controlled only by the one differential amplifier which is gated on. No current is drawn through those load resistors by the B Channel differential amplifier during the time the A Channel is activated, because of the multivibrator emitter current control described above which allows only one amplifier to conduct at any time. When the input signal is positive, A5Q1 will conduct more heavily than A5Q2, and the current through A5R15 will be greater than that through A5R14. Thus, the base of A5Q8 is driven less positive than the base of A5Q7, and A5Q7 will conduct more heavily than A5Q8. The current through A5R24 will be greater than that through A5R25, so that the differential output taken between A5-N and A5-C is positive at pin C with respect to pin N. This produces downward deflection of the CRT trace which is proper for a condition where a positive output is developed in the summing amplifier. (Because of the polarity inversion in the summing amplifier, a condition which should drive the trace downward, i.e. where gain offset exceeds the gain ratio, produces a negative input current to the summing amplifier and a positive output voltage.)

When zero input signal exists, A5Q1 and A5Q2 conduct equally, and the output signal drives the output amplifiers A5Q7 and A5Q8 to equal conduction at a level that supplies equal output of ≈ 0 V on each differential line.

Resistors A5R11 and A5R12, connected across the emitters of the differential amplifier pair, provide emitter degeneration for the amplifier. A5R11 adjusts the amount of degeneration and thereby sets the amplifier gain. A5R9 provides a balance adjustment to divide the constant-current emitter drive from the gating transistor A5Q3 to provide equal response from the differential transistors so that equal output signals are provided when the input at A5-A is 0 V. A5R2 provides an additional adjustment that sets the base bias of A5Q1 to the proper value to assure zero output when no signal is applied to A5Q1, thereby enhancing performance of the stage in amplifying low-level drift offset signals during manual balancing. A control similar to A5R2 is not required for the B Channel since that channel is not used for drift balancing operations. The balancing action provided by A5R20 is sufficient to zero-set the differential output in response to signals from the high-impedance output of the B Channel summing amplifier.

4.2.4.4 AC Blanking Signal Generator. Diodes A5CR2 and A5CR4 are used to tap off a trigger signal from the multivibrator circuit to drive the blocking oscillator circuit which generates the ac blanking signal. Each of these diodes is cut off when the transistor to which it connects is not conducting, since both leads of the diode are then returned to -12.6 V.

When the connected transistor starts to conduct, its collector is raised nearly to ground level, turning on the diode and producing a positive-going pulse at the diode cathode. When the connected transistor is cut off, a negative-going pulse is similarly produced at the diode cathode. The pulses developed at each diode cathode are coupled to a common trigger line for the blocking oscillator by A5C7 and A5C10. Since turn-on of one multivibrator transistor slightly precedes turn-off of the other multivibrator transistor, the trigger pulse train consists of a positive-going pulse at the start of each inter-channel switching interval, followed by a negative-going pulse at the end of each switching interval, with an interval of about 1 μs between pulses.

The blocking oscillator circuit operates to develop a 20 V pulse during the 1-μs switching interval between the two trigger pulses. A triggered blocking oscillator circuit is chosen because it is ideal for generating short pulses of large magnitude. The blocking oscillator transistor, A5Q11, is held at cut-off when no positive trigger pulses are applied, because the base and emitter are both returned to decoupled -12.6 V through resistors (A5R34 and A5R35).

When the positive leading segment of the trigger pulse is applied to the base of A5Q11, the transistor begins to conduct. Collector current flows through winding 2-1 of the blocking oscillator transformer, A5T1, and produces a varying magnetic flux that induces a voltage of the same polarity across winding 5-6. This induced voltage provides regenerative feedback by dropping the emitter voltage and thereby increasing the base-emitter forward bias until the transistor is driven into saturation and collector current ceases to increase.

When collector current is no longer increasing, no varying magnetic flux is generated to induce a regenerative feedback voltage across winding 5-6. The absence of this voltage, and the fact that the positive portion of the trigger pulse has passed, leaves A5Q11 biased to cut-off. When the collector current stops flowing, the collapsing field around transformer winding 5-6 tends to induce a voltage in winding 1-2 that is positive at terminal 1 with respect to terminal 2. Clamping diode A5CR5 shunts this induced voltage through R36 to prevent transistor breakdown. The negative trailing segment of the trigger pulse applied to the A5Q11 base reinforces the cut-off mode but otherwise serves no function.

The output of the blocking oscillator is obtained from winding 3-4 of A5T1. The initial current build-up in winding 2-1 induces a voltage in winding 3-4 that is positive at terminal 4 with respect to terminal 3. This voltage is coupled out to the Model 8000 via A5CR6 and A5-T. It has an amplitude of about +20 V and a pulse duration of about 1 μs. The opposite-polarity voltage developed when the field collapses is isolated from A5-T by the clamping action of A5CR6.

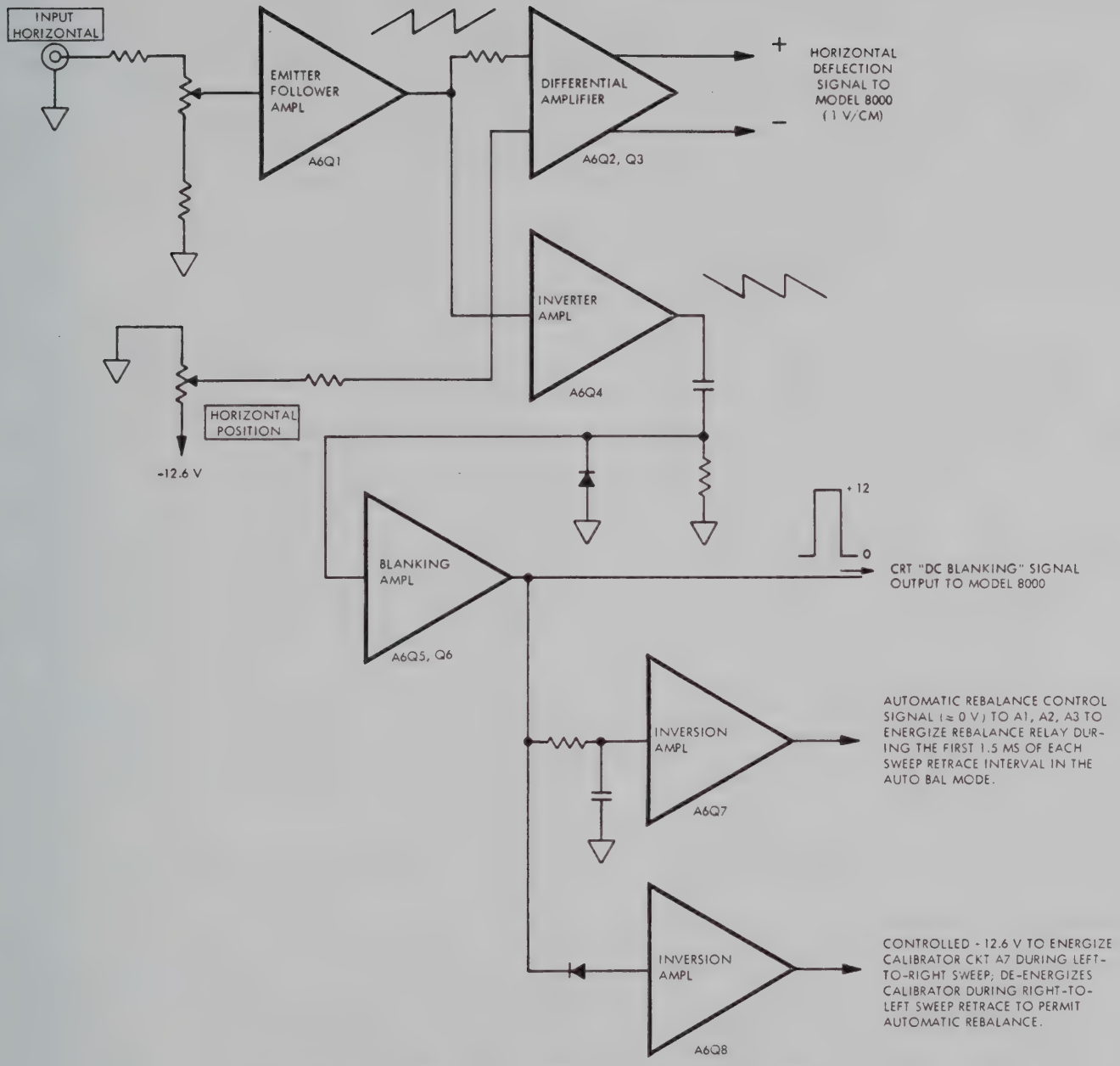

INPUT HORIZONTAL
EMITTER FOLLOWER AMPL
A6Q1
DIFFERENTIAL AMPLIFIER
A6Q2, Q3
+
–
HORIZONTAL DEFLECTION SIGNAL TO MODEL 8000 (1 V/CM)
INVERTER AMPL
A6Q4
HORIZONTAL POSITION
-12.6 V
+12
0
BLANKING AMPL
A6Q5, Q6
CRT "DC BLANKING" SIGNAL OUTPUT TO MODEL 8000
INVERSION AMPL
A6Q7
AUTOMATIC REBALANCE CONTROL SIGNAL (≈ 0 V) TO A1, A2, A3 TO ENERGIZE REBALANCE RELAY DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL IN THE AUTO BAL MODE.
INVERSION AMPL
A6Q8
CONTROLLED - 12.6 V TO ENERGIZE CALIBRATOR CKT A7 DURING LEFT-TO-RIGHT SWEEP; DE-ENERGIZES CALIBRATOR DURING RIGHT-TO-LEFT SWEEP RETRACE TO PERMIT AUTOMATIC REBALANCE.

FIGURE 4-9. BLOCK DIAGRAM OF SWEEP CIRCUIT (PART OF A6)

4.2.5 SWEEP CIRCUIT (HORIZONTAL AMPLIFIER AND RETRACE CONTROL CIRCUIT). (See Figure 4-9 and Schematic 900827C.) The sweep circuit components, shown in Figure 4-1 as the horizontal amplifier and retrace control circuit, supply the horizontal control signals for the Model 8000 oscilloscope. The horizontal amplifier (A6Q1 - A6Q4) amplifies an externally supplied sweep signal or an internally developed line-frequency sweep signal. The internal sweep is provided for calibration and balancing operations, and for single-frequency measurement applications.

The internal or external sweep is applied to input emitter follower stage A6Q1, which drives one input of differential horizontal amplifier A6Q2/A6Q3. The dc bias from the HORIZONTAL POSITION control is summed with the sweep signal at the base of A6Q2. A positive-going external input signal drives the differential output to move the trace from left to right.

The retrace control circuit, A6Q5 through A6Q8, senses the negative slope of the horizontal sweep signal during sweep

retrace, and generates a "dc blanking" signal which is maintained for the full retrace interval, and which is used to blank the CRT trace during sweep retrace. The retrace control circuit also generates two other output signals independent of the dc blanking signal but coincident with it in time. These signals are used to (1) energize relay K1 in A1/A2/A3 to establish automatic rebalancing during the first 1.5 ms of each sweep retrace interval when operation in that mode is selected, and (2) remove power from the RF Calibrator circuit so that it complies with the "full off" signal output requirement during retrace to permit use of automatic drift rebalancing in the calibration mode.

In the retrace control circuit, A6Q4 is an inverting amplifier and the voltage on its collector has a positive slope during retrace when the input signal has a negative slope. The rising voltage on the collector of A6Q4 causes a current flow in differentiating capacitor A6CR1, thereby turning on A6Q5 and A6Q6 to generate the "dc blanking" pulse which blanks the Model 8000 CRT retrace. The turn-on of A6Q6 de-energizes A6Q8, removing +12.6 V power from the calibrator circuit to eliminate the calibrator rf output during retrace. (This permits use of automatic rebalancing in the CAL mode.) The turn-on of A6Q6 also applies a positive signal to the base of A6Q7, turning on that transistor to complete the ground-level control signal to the rebalance relays in A1, A2, and A3 when the BALANCE switch is in the AUTO position. Differentiating capacitor A6C5 shortens the interval during which a positive signal is applied to the base of A6Q7 to 1.5 milliseconds, regardless of the duration of the retrace interval, by charging to the cut-off level of A6Q7 during the first 1.5 milliseconds.

During the forward portion of the sweep, the negative-going signal at the collector of A6Q4, and the resulting differentiating capacitor current in A6C2, turns off A6Q5 and A6Q6 to remove the retrace blanking signal. When A6Q6 cuts off, the base of A6Q8 is returned to a near-ground potential, turning A6Q8 on to supply +12.6 V power to the rf calibrator circuit.

4.2.5.1 Detailed Theory of Sweep Circuit. The individual circuits of Sweep Circuit PC Board A6 are discussed in detail below. Circuit waveforms are shown in Figure 5-6 (page 5-18).

4.2.5.2 Horizontal Amplifier Circuit. The horizontal input signal supplied at A6-B controls the conduction of emitter follower A6Q1. When the instrument is operated in the External Sweep mode, the sweep drive signal applied to the INPUT HORIZONTAL jack is tapped at a variable point in the R2/R3/R4 input voltage divider by HORIZONTAL SENSITIVITY control R2. With no input signal, the base of A6Q1 is returned to ground level through R2 and R4, and a minimum level of conduction is established. When a positive sweep drive voltage is applied, Q1 conducts more heavily, and its output voltage at the emitter junction with load resistor A6R1 becomes increasingly positive with a linear relationship to the input signal.

The output of emitter follower A6Q1 provides a low-impedance drive to A6Q2 in the horizontal amplifier differential pair. This horizontal input signal is summed at the base of A6Q2 with a fixed-voltage signal developed by the HORIZONTAL POSITION control R5. The remaining stage of the differential pair, A6Q3, has its base fixed at ground level. Resistor A6R5 applies some negative feedback to the differential amplifier input to stabilize the gain and response of the stage. When the sum of the voltage supplied by the HORIZONTAL POSITION pot and the input emitter follower is 0 V, A6Q2 and A6Q1 conduct equally and the output of each collector is identical and ≈0 V. The differential output between A6-C and A6-H is therefore 0 V, as required to center the spot horizontally on the CRT.

If the HORIZONTAL POSITION control is turned CCW, and/or the input signal voltage decreases, an increasingly negative voltage is applied to the base of A6Q2, decreasing its conduction so that pin A6-C becomes positive with respect to A6-H. This drives the trace to the left side of the CRT. If the HORIZONTAL POSITION control is turned CW, and/or the input signal voltage increases, an increasingly positive voltage is applied to the base of A6Q2, increasing its conduction so that pin A6-C becomes negative with respect to A6-H. This drives the trace to the right side of the CRT.

Normally, the HORIZONTAL POSITION control is set to supply a voltage which, when summed with the quiescent output of A6Q1, places the spot 5 cm left of CRT center. The HORIZONTAL SENSITIVITY control is then set so that the maximum sweep input voltage, summed with the HORIZONTAL POSITION control output, places the spot 5 cm right of CRT center.

When the INTERNAL SWEEP mode is used, a 3.15 VAC signal is applied to the base of A6Q1. This signal is tapped from 6.3 VAC by voltage divider R6/R7. This signal varies the conduction of A6Q1 both above and below the quiescent level, and with a proper setting of the HORIZONTAL POSITION control, will provide a full-screen sweep.

4.2.5.3 D.C. Blanking Circuit. The output of emitter follower A6Q1 in the horizontal amplifier supplies an impedance-converted output of the internal or external horizontal sweep drive signal to inverting amplifier A6Q4 for the dc blanking circuit. During retrace when the horizontal input signal at A6-B has a negative slope, the base drive applied to A6Q4 also has a negative slope, and its conduction decreases. This decreases the current through load resistor A6R11, producing an output voltage with positive slope at the A6Q4 collector.

A6C2 and A6R14 constitute a differentiating circuit that draws a current through A6R14 proportional to the voltage slope of the A6Q4 positive ramp output. This current establishes the necessary base-emitter bias on A6Q5 to saturate that transistor, and the resulting load current through A6R15 and A6R16 also causes A6Q6 to saturate. The heavy conduction of A6Q6 produces a signal of ≈+12 V at A6-V, which serves as the dc blanking signal to drive the H.V. Regulator & Blanking P.C. Board A11. Note that the differentiating action of A6C2/A6R14 provides a positive saturation drive to A6Q5 only during the retrace interval when a positive ramp output is supplied by A6Q4. During the forward sweep and the "waiting period", if any, before a sweep starts, the output of A6Q4 has either a negative slope or zero slope, neither of which produces positive current through A6R14 to ground, and A6Q5 and A6Q6 are thus turned off. This differentiator-controlled saturation of A6Q5 and A6Q6 provides the "full-on" or "full-off" response which gives the dc blanking signal output its excellent pulse shape.

R-C Coupling Network A6C1/A6R10 provides improved frequency response in the inverting amplifier stage, and feedback network A6R12/A6C9 provides negative feedback that improves stability. A6CR1 prevents negative current from being drawn through A6R14 when the differentiator responds to the negative

ramp output, and thereby protects the emitter-base junction of A6Q5 against reverse breakdown. A6CR2 clamps the output at ground level to prevent negative overshoot on the falling edge of the dc blanking pulse output.

4.2.5.4 Automatic Rebalance Control Signal. Voltage divider A6R18/A6R19 applies a portion of the +12 V dc blanking signal to a differentiator circuit consisting of A6C5 and A6R22. During the first 1.5 ms of each dc blanking pulse, sufficient charging current is drawn through A6R22 to provide a positive base drive for A6Q14 and A6Q7, which constitute a Darlington amplifier stage. (In units below serial no. 121, A6Q7 is used alone.) The positive signal saturates the amplifier A6Q14/A6Q7, effectively connecting A6-L to ground to complete the return path for the rebalance relay energizing circuit.

After 1.25 ms (somewhat less in circuits with A6Q7 alone), capacitor A6C5 has charged to the point where its differentiator action is diminished and insufficient current is drawn to forward-bias A6Q14/A6Q7. Then A6Q14/A6Q7 cuts off, removing the ground connection from A6-L and de-energizing the automatic rebalance relay. A6CR3 clamps the base of A6Q14 to ground level to prevent negative overshoot when A6C5 responds to the negative-going end of the dc blanking pulse.

4.2.5.5 RF Calibrator Control Signal. The dc blanking signal output is coupled to A6Q8 through A6R20 and A6CR4. During the interval when the +12 V dc blanking pulse is supplied, A6CR4 is back-biased to isolate the base of A6Q8. This cuts off A6Q8, removing +12.6 V power from the rf calibrator to de-energize it during sweep retrace, thereby meeting the "rf off" criteria required for automatic balancing during retrace in the calibration mode.

During the quiescent period after the retrace is completed, and during forward sweep operation, whenever the +12 V dc blanking pulse is not present at A6-V, the output line is returned to a below-ground level by voltage divider A6R17/A6R18/A6R19. This negative bias is coupled to the base of A6Q8 to produce saturation, so that the +12.6 V from A6-S is coupled to A6-T to energize the rf calibrator.

4.2.6 RF CALIBRATOR CIRCUIT. (See Schematic 900823D.) The calibrator circuit, contained in shielded Module A15 of the plug-in unit, consists of a shielded and stabilized, 30-MHz oscillator with a precision ladder attenuator that establishes output levels in 10-db increments between -40 dbm and +20 dbm. The 30 MHz oscillator delivers 100 mw into 50 ohms. This 100 mw level is accurate to ± 0.3 db over the full operating temperature range of the instrument. The 0 to 60 db resistive ladder attenuator is accurate to within ± 0.3 db. The internal calibration oscillator is modulated by a blanking pulse coincident with the "dc blanking" signals so that automatic balancing may be used during the calibration procedure.

4.2.6.1 Detailed Theory. A transistorized Class C Colpitts oscillator is used to supply the rf calibration signal output at approximately 30 MHz. A7Q1 is the oscillator transistor, and A7C3, A7C5, and A7L4 constitute the 30 MHz tank circuit. The output signal is capacitively coupled to the step attenuator circuit by A7C4. Regenerative feedback to the base of A7Q1, 180° out-of-phase with the output at the collector, is supplied by A7C2. Operating power of +12.6 V dc is supplied from J6-T except during sweep retrace. L-C filters A7L1/A15C1 and A7L3/A15C2 prevent the 30 MHz signal from coupling out into the dc power circuits.

The Class C oscillator develops peak-to-peak voltage output approximately equal to twice the dc supply voltage. The Power Cal. control A7R1 controls oscillation amplitude by setting the effective collector-to-emitter supply voltage available across A7R2 and A7R4. Collector bias is obtained through A7L2 from the junction of A7R1 and A7R2, and this voltage is stabilized by A7C1. The base is connected to near ground by level C of the CALIBRATOR step attenuator control when in the OFF position, to disable the oscillator stage. In all other positions, base bias is obtained from the A7R2/A7R4 voltage divider.

A7C7 is the emitter bypass capacitor, and A7C6 acts as a high frequency bypass capacitor for the feedback applied at the A7Q1 base, to prevent high-frequency harmonics from excessively distorting the Class C amplifier output. Hence, regenerative feedback is applied to the base only for the 30 MHz fundamental. Thus, higher harmonics are suppressed in the oscillator output to more than 60 db below the fundamental. This assures that the CALIBRATOR output signal at any DBM level is sufficiently free of harmonic distortion to be within the specified accuracy (Table 1-1), even though higher harmonics are not attenuated the same as the fundamental by the output attenuator because of rf coupling effects.

The CALIBRATOR step attenuator A15S1 has 8 positions to provide 7 discrete DBM levels (-40 DBM to +20 DBM) and OFF. The switch applies the output from A7Q1 to various points in a ladder attenuator consisting of resistors A15R1 through A15R14, and also taps off a signal for the OUTPUT CALIBRATOR jack from other points in the ladder. Resistor values and tap connections are arranged so that the series and parallel combinations of resistors between each input and output connection point and ground are arranged to constitute a pi or L-pad which provides the specified output level with an output impedance of 50 ohms. In the +20 DBM position, the A7Q1 output is applied directly to the OUTPUT CALIBRATOR jack in parallel with 1 K resistor A15R15. The impedance of the oscillator output circuit combines with A15R15 to provide the proper 50-ohm level.

4.2.7 OVEN ASSEMBLY MODULE. (See Schematic 900823D.) This module is mounted on the bottom of the Model 7051 Plug-in. It serves to maintain a constant-temperature environment for the sensitive low-level differential input transistors A8Q1, A8Q3, and A8Q5 and also the temperature-dependent logarithmic feedback transistors A8Q2, A8Q4, and A8Q6, which function in the log converter amplifier circuit. The cans of these transistors are physically mounted inside holes in the copper heat sink block of the oven and thus are maintained at a constant temperature and insulated against thermal shock. The oven temperature is held constant at about 55° C by a thermistor-controlled regulator circuit contained on Sweep PC Board A6 (See Figure 4-10). In this circuit, the temperature regulator amplifier (A6Q9 - A6Q11) drives the heater transistor A8Q7 which is mounted on the oven heat-sink block. Thermistor A8RT1 is the temperature-sensing thermistor which drives the regulator circuit, and A8RT2 compensates for the temperature characteristic of v_{be} in A8Q7. Amplifier A6Q12 and A6Q13 and storage capacitor A6C7 control the OVEN TEMP STABILIZED light, turning it on when the oven temperature has stabilized with a low level of "temperature-maintenance" current through A8Q7.

4.2.7.1 Detailed Theory of Oven Heater Circuit. A separate full-wave, filtered, unregulated dc power supply is provided for the oven heater circuit. This supply, consisting of CR1-4, C1 and R1, develops about 36 V, and is protected by fuse F1. The output of the supply provides operating current for oven heating transistor A8Q7. This transistor is tightly attached to the copper

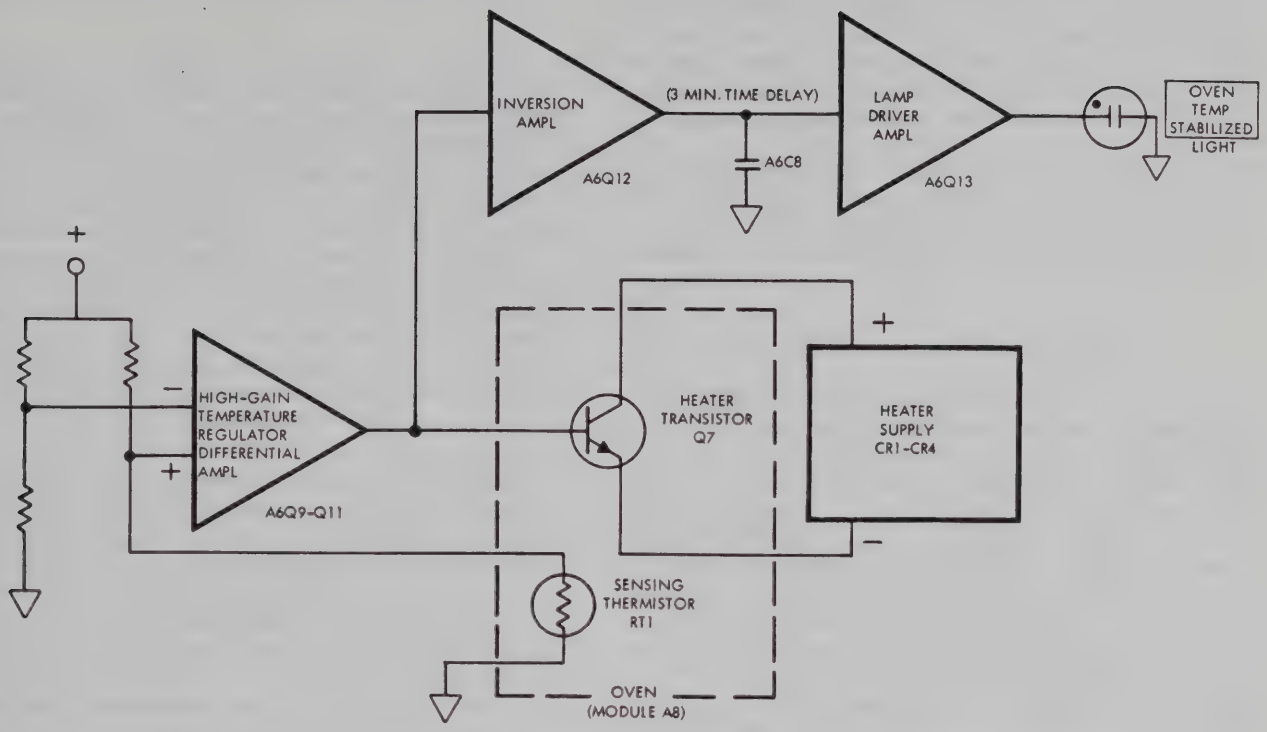


FIGURE 4-10. BLOCK DIAGRAM OF TEMPERATURE REGULATOR CIRCUIT (PART OF A6)

heat sink block of the oven and maintains the oven at a constant temperature by dissipating a controlled amount of power, as required to offset heat loss to maintain the oven at about +55° C. Thermistor A8RT2, also mounted on the oven block, provides temperature sensing for driving the temperature regulator amplifier.

4.2.7.2 Detailed Theory of Temperature Regulator Amplifier. The resistance of A8RT1, compared to that of A6R31, establishes the operating condition of differential input stage A6Q9, A6Q10 of the temperature regulator amplifier contained on Sweep PC Board A6. These components, plus A6R23 and A6R28, constitute a bridge circuit which controls the differential stage. A8RT1 has a resistance of 1 K at the proper operating temperature (≈ 55° C), thereby balancing the circuit. When the oven is below operating temperature, the resistance of A8RT1 increases and biases A6Q9 to heavier conduction. When the temperature rises above operating level, the resistance of A8RT1 decreases and reduces the conduction of A6Q9. Resistors A6R26 and A6R27 provide emitter degeneration in the differential amplifier circuit to regulate the gain.

The differential amplifier output drives amplifier stage A6Q11 which controls the oven heating transistor A8Q7. Output current from A6Q11 is limited by A6R30, which with A6R32 constitutes an output divider for the base current driving A8Q7, with the result that maximum current in Q7 is limited to about 1 ampere. Thermistor RT2 provides over-temperature protection by decreasing its resistance to the point where Q7 is biased to cut-off if the temperature reaches +100° C.

At initial turn-on, when temperature is low and the bridge unbalance biases Q9 to conduct heavily, the increased drop across A6R24 biases A6Q11 to heavy conduction. This increases the signal applied to A8Q7, causing it to conduct heavily and generate more heat per unit time than the oven dissipates through heat loss, thereby increasing the oven temperature. There is some thermal conduction lag in the response of A8RT1 and, thus, in the regulator loop, with the result that the maximum oven heater current is maintained until the oven reaches operating temperature, after which the current temporarily drops to zero as the regulator attempts to correct the temperature overshoot. After a period of several seconds, the temperature starts to drop again, and the A8Q7 collector current builds up to about 120 ma and then oscillates slowly around the proper steady-state value of about 60 ma, and stabilizes at that value after a few minutes.

4.2.7.3 Operation of OVEN TEMP STABILIZED Light. The control circuit for the OVEN TEMP STABILIZED Light prevents turn-on of that light during the initial period of temperature fluctuation in the oven. When A6Q11 is biased to heavy conduction to heat the cold oven, the junction of A6R29 and A6R30 is raised to almost +12.6 V. This drives A6Q12 to heavy conduction, dropping the junction of A6R34 and A6R36 to ground level, and thereby back-biasing A6Q13 to cut off and open the return circuit of DS1. Capacitor A6C7 adds a time delay to the coupling circuit between A6Q12 and A6Q13, so that the positive-going transients that occur during the oscillations of oven heater current when approaching operating temperature do not turn on A6Q13. When steady-state conditions are reached, the low current through A6Q11 causes its collector to operate <2 V above ground, so that the A6R29/A6R33 divider, returned to -12.6 V, cuts off A6Q12. A6CR5 prevents A6Q12 from being back-biased too far. When the current in A6Q12 drops to zero, A6C7 begins charging toward +126 V through A6R34. After about 3 minutes, A6C7 has built up to above +12.6 V, and turns on A6Q13. After A6Q13 turns on, base current returning to the +12.6 V supply through A6Q13 stabilizes the A6C7 voltage at ≈+15 V. The turn-on of A6Q13 couples pin A6-P to +12.6 V, energizing OVEN TEMP STABILIZED light DS1. A6R35 and A6R38 form a voltage divider between +12.6 V and +126 V to

drop the voltage at pin A6-U to about +100 V so that the level applied to the A6Q13 collector through DS1 will not exceed +85 V.

When the OVEN TEMP STABILIZED light goes on, the instrument is ready for use, although a small amount of thermal instability continues for the first 15 minutes of operation. The only effect of this is that when the instrument is operated near the limit of its sensitivity and with manual balancing, the manual balance adjustment may have to be "touched up" slightly every five minutes or so during the first 15 minutes of operation. When automatic balance operation is used, the instrument is ready for use as soon as the OVEN TEMP STABILIZED light comes on, and no manual balance adjustments should be necessary. With manual balancing, if the instrument is properly balanced after a day's operation, and then is turned off, it can be expected to return to the same operating point with no manual balance readjustment within 15 minutes after the next turn-on.

4.2.8 FRONT PANEL CONTROLS. The DISPLAY Mode Selector switch, located on the left-hand center portion of the Model 7051 panel, makes a major contribution to the ease of operation of this instrument. A 12-position switch, its settings are labeled in four groups with three positions per group. The RATIO group of positions selects signal level ratios for display: either A or B Channel ratioed to the REF Channel or both ratios displayed simultaneously. The LOG group of positions selects the absolute signal level outputs of the A and B Channels to be viewed singly or simultaneously. When the DISPLAY Mode Selector switch is in any of the three LOG positions, the output of the REF log converter amplifier is disconnected from the channel summing amplifiers so that ratios are not taken.

The BALance group of positions is used to permit fast, simple manual balancing of the log converter amplifiers. When in the BAL mode, the internal sweep is automatically energized, the summing amplifiers are bypassed, and the output of the log converter amplifier being balanced is connected directly to the Display Switch (chopper) circuit, which operates in a single-channel display mode. When balancing a log converter amplifier, one desires 0 V output for 0 V input. With the DISPLAY Mode Selector switch in any of the balance positions, and with the channel being balanced having 0 rf input, 0 output occurs when the horizontal trace is directly at the center of the CRT. If the channel log amplifier is out of balance, it will be indicated by a non-centered position of the CRT trace. The amplifier may then be brought into balance by adjusting the screwdriver BALance control on the front panel directly above the channel input jack to position the trace exactly in the center of the CRT.

The CALibrate group of switch positions is used when it is desired to adjust or check the calibration of the instrument and/or the crystal detectors being used. When calibrating the instrument, one merely matches the specific logarithmic converter amplifier to the specific crystal detector. As discussed previously, all commonly used crystal detectors have a uniform response curve shape through the square law, transition and linear regions. The only difference from crystal to crystal is the level at which the departure from the square law occurs. When calibrating a crystal, the technique is to inject a signal which is switched between -20 dbm and +10 dbm (square law to linear law) and adjust the gain-changing compensation in the log converter amplifier such that the calibrated readout of the Model 7051 indicates a 30 db change. The level at which the compensation begins is adjusted by a panel control for each channel labeled +10 CAL. It is located above the BALance control of the same channel. Since the potentiometer operated by the +10 CAL control has little effect at -20 dbm, it is adjusted while +10 dbm is applied to the crystal detector.

In the lower center of the Model 7051 panel, the OVEN TEMP STABILIZED lamp indicates when the internal oven temperature has stabilized and at the correct temperature. No measurements should be taken with the Model 7051 unless this lamp is lit.

4.3 CIRCUIT DESCRIPTION OF OSCILLOSCOPE.

4.3.1 PRIMARY POWER DISTRIBUTION. (See Schematic 900804D.) The power input through the line cord pases through the main fuse F1 on the rear of the chassis. From the POWER switch S1, the power connects to transformer T1 and to the plug-in unit connector J1. The line power to J1 is not used by the Model 7051 Plug-in unit. The connection to the T1 primary windings is made through 115-230 VAC switch S2 located inside the rear of the chassis at the bottom. S2 is arranged so that for 115 V operation, the two windings are connected in parallel; while for 230 V operation they are connected in series. Thus, in either mode of operation, 115 V power is applied to each winding. The 115 V applied to one winding is used to drive the POWER ON light DS1. The 115 V applied to the other winding is also used to supply 115 V to connector J1-22. This 115 V ac input is not used by the Model 7051 Plug-in unit. The voltage outputs from T1 are utilized to drive the power supplies and oven heater circuit.

4.3.2 LOW VOLTAGE SUPPLIES. (See Schematic 900805C.) The Low Voltage Supplies, all contained on PC Board A13, provide -12.6 V dc (A13Q8-A13Q10 and Q3 on main chassis); +12.6 V dc (A13Q5-A13Q7 and Q2 on main chassis); and +126 V dc (A13Q1-A13Q4 on Q1 on main chassis). The zener-regulated -12.6 V supply is the primary reference for the other supplies and for all instrumentation circuits in the instrument. AC outputs of 6.3 V for CRT filament and internal sweep drive, and 26.2 V for driving the oven heater transistor circuit are also provided.

4.3.2.1 Detailed Theory of -12.6 V Supply. The -12.6 V supply consists of a two-stage amplifier (differential amplifier A13Q9/A13Q10 and an emitter-follower driver A13Q3) and a series regulator transistor (Q3). The components shown within the dotted border in Schematic 900805C, are located on L.V. Supply Circuit Board A13, accessible from the top of the instrument. The use of metal film resistors in all critical circuits, and matched transistors in the input differential stage, minimizes noise and drift in this supply. As in all closed-loop feedback systems, tight control of phase response must be maintained. This is accomplished by A13C7 and A13R19 located in the amplifier output stage, at the collector of A13Q8.

The feedback loop operates as follows to keep the output constant at -12.6 V: The primary reference standard is A13CR3, a 1N823 temperature-compensated zener diode, which controls the reference bias at the base of A13Q9 in the differential stage. If the output should tend to increase negatively to more than -12.6 V, the forward emitter-base bias on A13Q10 in the

differential stage, tapped between -12.6 V output and ground by voltage divider string A13R25/A13R26/A13R27, decreases below that of A13Q9. This is because A13CR3 holds the base voltage constant on A13Q9, while the output voltage divider drops the base voltage applied to A13Q10 when the -12.6 V output at A13-R drops. A13Q9 then conducts more heavily, and the drop across A13R20 couples a more negative signal to the base of A13Q8. This will, in turn, decrease the conduction of A13Q8 which tends to make its emitter less positive.

This action decreases the forward bias and therefore the conduction of regulator transistor Q3 so that it offers greater series resistance, returning the level to exactly -12.6 V. The regulator transistor is connected between the + terminal of the full-wave rectifier (CR5 - CR8) and ground. Thus, the increased series resistance it offers when conduction is decreased produces an increased reverse-polarity voltage drop between the rectifier + terminal and ground. This increased drop "bucks" the rectifier voltage by moving its + tie point further above ground, thereby making the output less negative. If the output should tend to becomes less negative than -12.6 V, the feedback loop will restore the output level by increasing the conduction of Q3. The -12.6 V output is connected to TP5 on the top of the instrument. Potentiometer A13R26 permits precision adjustment of the -12.6 V output by establishing the proper quiescent operating bias for A13Q10. Since the -12.6 V supply serves as primary reference for the instrument, it must be set to -12.60 V ± 0.01 V.

4.3.2.2 Detailed Theory of +12.6 V Supply. The -12.6 volt supply output is applied to A13R17 in the +12.6 V supply to serve as a reference for the +12.6 V supply. Except for the reference circuit, the +12.6 V supply circuitry is similar to the -12.6 V supply. The +12.6 V output, applied to A13R16, and the -12.6 V reference applied to A13R17, provide a voltage-divider drive of ≈ 0 V for the base of A13Q7 in the differential amplifier stage. The base of A13Q6 is returned to ground through A13R15, which balances the offset in the A13R16/A13R17 voltage divider produced by A13Q7 base current through A13R16.

A13Q5 is the driver stage, and Q2 is the series regulator transistor. Q2 is located in the + output line, so that the variable drop due to its controlled series resistance regulates the output voltage directly.

4.3.2.3 Detailed Theory of +126 V Supply. This supply also uses a voltage divider string between its output and -12.6 V to sum the reference and feedback signal for regulator control. A13R9 through A13R11, with A13R12, comprise the voltage divider between +126 V and -12.6 V. The voltage divider output of ≈ 0 V is applied to the base of A13Q4 in the amplifier differential input stage. The base of A13Q3 in the differential pair is connected to ground through A13R5. Diodes A13CR1 and A13CR2 limit the input signal excursions applied to A13Q4.

Common-base amplifier stage A13Q2 provides the necessary voltage gain to operate the emitter-follower driver stage A13Q1. The base of A13Q2 is tied to +12.6 V, and collector bias is supplied by A13Q1 base current through A13R1.

The amplifier operates as follows to keep the output voltage constant at +126 V: If the output should tend to increase positively, increased positive bias would be applied to the base of A13Q4, increasing the conduction of that side of the differential amplifier. The increased current through R6 drops the voltage on the emitter of A13Q2, increasing the forward bias and collector current through that transistor.

The increase in collector current in A13Q2 produces a corresponding increase in base current in A13Q1 which, in turn, increases the emitter-collector current in A13Q1. The A13Q1 emitter is returned to the most positive point in the output circuit of rectifier CR9-CR12. With low emitter current, A13Q1 has its emitter biased more positively than its collector, which is tied to the +126 V bus, so that regulator transistor Q1 is forward-biased for heavy conduction. Increased conduction of A13Q1 reduces its emitter voltage closer to that of the collector, which thereby reduces the forward bias on regulator transistor Q1. This increases the series resistance of Q1 to offset any tendency for positive increase in the output voltage.

If the output should tend to decrease to less than +126 V, the feedback amplifier loop will restore the output level by increasing the conduction of Q1. The regulator amplifier phase response characteristic is controlled by A13C1/A13R4 in the output driver stage and A13R5/A13C2 in the input differential amplifier stage. A 1-ohm resistor, R14, is connected between the +126 V bus and the regulated output filter capacitor C1-B, to prevent supply oscillation.

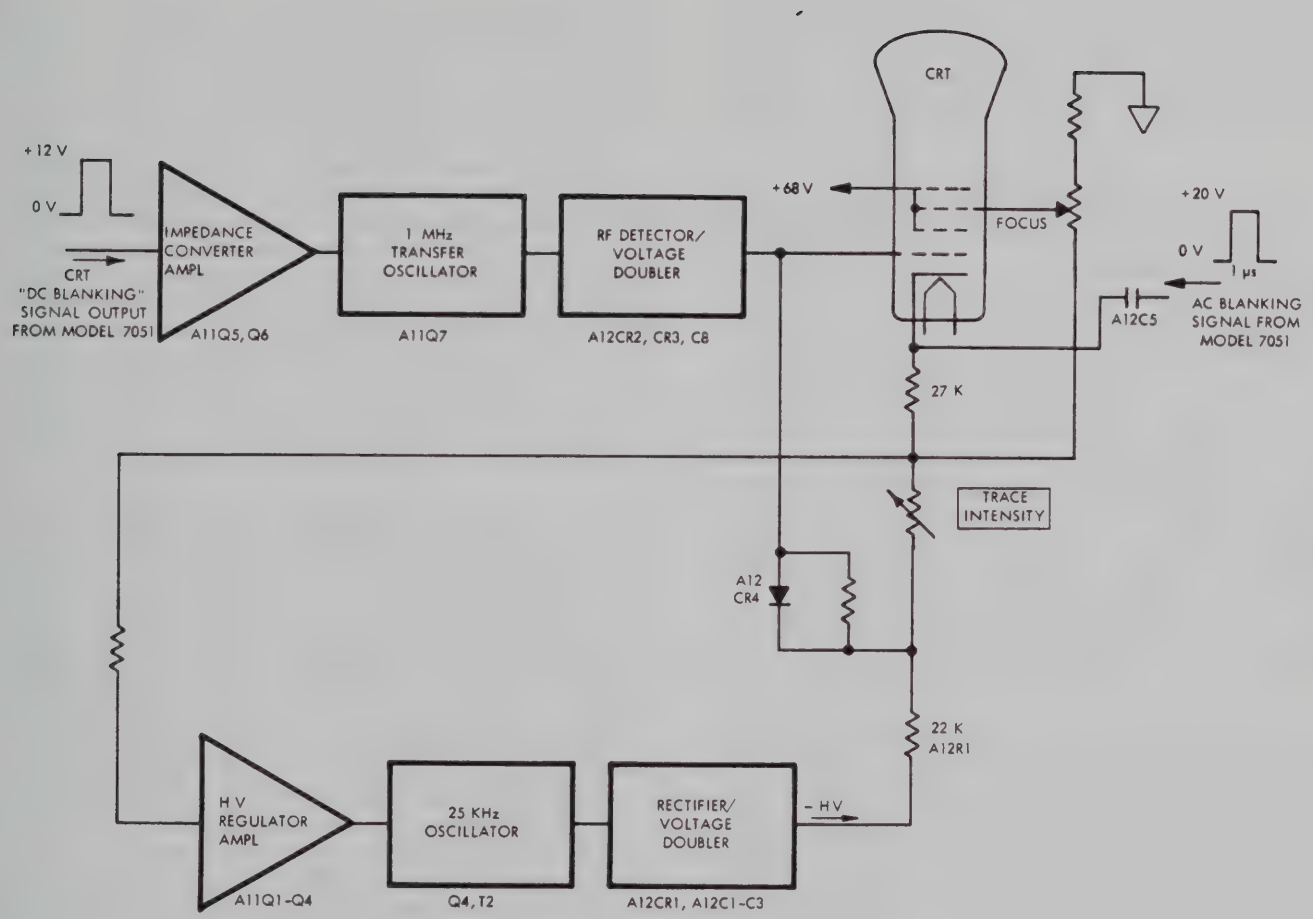


FIGURE 4-11. BLOCK DIAGRAM OF H V SUPPLY, REGULATOR, AND BLANKING CIRCUITS (A11, A12)

4.3.3 HIGH VOLTAGE SUPPLY, RECTIFIER, AND REGULATOR CIRCUITS. (See Figure 4-11 and Schematics 900804D and 900807C.) The High Voltage Supply consists of a 25 KHz oscillator stage (Q4) and output step-up transformer T2. The High Voltage Rectifier circuit, contained on PC Board A14, rectifies the H V Supply output and provides proper voltage taps to drive the electron gun elements of the CRT. A14 also includes a voltage-dropping resistor string that provides a low-voltage drive to the H V Regulator and Blanking Circuit contained on PC Board A11. The regulator amplifier consists of a 4-stage amplifier (A11Q1 - A11Q4) which controls the base current of the oscillator transistor Q4 in the H V Supply, to control the level of oscillation and thereby regulate the high voltage output.

4.3.3.1 Detailed Theory of High Voltage Supply. In the circuit of oscillator Q4, a filter circuit consisting of L1, L2, and C4 is used to prevent rf coupling from the 25 KHz oscillator onto the + and -12.6 V dc supply lines. Winding 3-4 on transformer T2, a "tickler" winding the equivalent of one turn, but consisting of two loops of high voltage insulated wire wrapped around one half of the T2 core, provides positive feedback to Q4 to stimulate and maintain oscillation. The 20-turn primary winding (winding 5-6) couples the Q4 oscillations to the T2 core, and is resonated by C7. Capacitors C8 and C9 provide rf bypass in the base-emitter circuit, and R6 stabilizes the base-emitter bias of Q4 at a point which prevents relaxation oscillation and permits control of oscillation amplitude by the base drive current input from the Regulator Amplifier (PC Board A11). Coupling resistor R5 protects transistor Q4 from voltage surges in the base drive signal.

4.3.3.2 Detailed Theory of H.V. Rectifier and Distribution Circuits. The high voltage ac output from the HV supply oscillator is obtained from the 1250-turn secondary winding on T2. It is rectified by dual-diode A12CR1 whose output is connected to high voltage capacitors A12C1 and A12C2 to form a voltage-doubler output circuit. A12R1 and A12C3 form a high voltage output filter, essentially eliminating the 25 KHz ripple from the high voltage dc. The CRT grid bias line is connected to the output of A12C3, as required to make the grid the most negative electrode in the tube.

Intensity Limit adjustment A12R2 provides a series drop in the output voltage to assure a reasonable range for the front panel TRACE INTENSITY control. The TRACE INTENSITY control sets the hv output supplied to the CRT cathode. This voltage is connected directly to the heater, and coupled through A12R15 to the cathode of the CRT. A12R15 provides a drop to assure that the cathode is biased positively with respect to the heater, to avoid discharge of electrons in the wrong direction. Anode 1 (the focus electrode) of the CRT requires a voltage that is 300 V positive with respect to the cathode, and draws essentially no current. This is supplied by a voltage divider between the hv supply output and ground, consisting of Focus resistor A12R4 and series resistors A12R3 through A12R9. The focus electrode bias is set by adjusting A12R4. Since both A12R2 and A12R4 are operated at high voltage, an insulated screwdriver must be used to adjust them. The positive bias for anode 2 of the CRT is obtained from voltage divider A14R26 and A14R27 tapped between the +126 V and +12.6 V supplies.

4.3.3.3 Detailed Theory of High Voltage Regulator. The regulator circuit in A11 includes a differential input stage (A11Q1, Q2) in which the input to A11Q1 consists of a summation of a positive reference current fixed by the +12.6 V supply level (coupled through A11R1) and a negative feedback current proportional to the (-) high voltage supply output, tapped from a divider string consisting of A12R10 through A12R14. This divider string drops the voltage from ≈ -2500 V at pin 11 of A12 to essentially ground level at pin 5. Resistors A12R10 through A12R14 and A11R1 all are metal-film type to provide uniform temperature-compensation of both feedback resistance paths. The base of A11Q2 is returned to ground, so that the differential stage is balanced when the negative high voltage feedback and the positive reference feedback cancel at the base of A11Q1. The output of the differential stage is amplified by A11Q3. A11R4 and A11C5 provide feedback compensation in the coupling circuit to A11Q3 to prevent low-frequency oscillations in the regulator. A11Q4 is the regulator output stage which controls the base-emitter bias in oscillator transistor Q4, and thereby regulates the oscillation amplitude and output voltage.

The level of conduction of A11Q4 controls the current from -12.6 V to ground through L2 and R6, thereby establishing the Q4 bias. When the HV supply output level is not sufficiently negative, A11Q1 is biased to conduct more heavily then A11Q2. The decreased conduction of A11Q2 reduces the forward bias on A11Q3. The reduced conduction of A11Q3 drops the base voltage of A11Q4 to cause it to conduct more heavily and drop the output voltage at A11-R. The resultant increased current through R6 increases the forward base-emitter bias on Q4 to increase the amplitude of the oscillations.

4.3.4 BLANKING CIRCUITS. (See Figure 4-11 and Schematic 900807C.) The "ac blanking" pulse from the plug-in is coupled directly to the CRT cathode via A12C5. The "dc blanking" pulse is amplified and impedance-converted on the HV Regulator and Blanking PC Board by A11Q5 and A11Q6 and raised to high-voltage potential by a transfer oscillator stage (A11Q7) for application to the grid of the CRT via a detector and voltage doubler circuit on the HV Rectifier PC Board (A12CR2, A12CR3, and A12C8).

4.3.4.1 AC Blanking Signal. The ac blanking signal serves to blank the 100 KHz switching transient between segments of the dual-channel presentation. This signal, consisting of a +20 V, 1-μs pulse developed on the Chopper PC Board A5, is coupled directly to the CRT cathode through A12C5. This positive signal increases the cathode - to - grid biasing potential to the point where the CRT trace is completely blank. Resistor A12R15 isolates the ac blanking signal from the low impedance of the hv supply output. Resistor A12R16 provides a ground return for A12C5 to eliminate build-up of high voltage on the ac blanking signal interconnection lines through capacitor leakage.

4.3.4.2 Detailed Theory of DC Blanking Signal. The dc blanking signal blanks the retrace portion of the presentation. To provide suitable blanking for the long retrace intervals associated with slow sweeps, a low-source-impedance, dc-coupled signal is required, since the signal must effectively "buck" the high voltage supply during the entire retrace period. The low-level dc blanking signal developed on Sweep PC Board A6 is amplified and raised to high voltage level by the circuit of A11Q5 through A11Q7 and A12C7 through A12R18. The dc blanking signal applied to A11-D is a positive pulse of +12 V, with a duration controlled by the sweep retrace time. Diode A11CR1 isolates the remaining dc blanking amplifier circuits from the effects of negative pulses. Transistor A11Q5 is a pulse amplifier. The collector output is developed across load resistors A11R7 and A11R8, while A11L1 serves as a peaking coil to provide fast rise time, and A11R12 provides the collector bias drop. A11R10 and A11R11 provide a feedback connection that serves to hold the collector of A11Q5 at a fixed potential of about +40 V by regulating the base voltage. The A11Q5 emitter is returned to ground.

The fast-rise leading and trailing edges of the (-) dc blanking pulse waveform are ac-coupled directly to the grid of the CRT from the A11Q5 collector by high voltage capacitor A12C6. To provide the dc drive power for the relatively long pulse, the collector output of A11Q5 is coupled to isolation amplifier stage A11Q6 which drives transfer oscillator A11Q7 that converts the dc signal to ac for coupling to the high voltage CRT bias circuit. In the transfer oscillator stage, A11L2 and A11C9 constitute the tank circuit, and A11C10, ten times as large as A11C9, couples a positive feedback signal to the base of A11Q7 via A11C8. Base bias for A11Q7 is provided by A11R19. Choke A11L3 and filter capacitors A11C6 and A11C7 prevent transfer oscillator signals from being coupled out to the power supplies or other circuits. A11R18 loads A11L3 to prevent ringing or spurious oscillations.

The transfer oscillator output is coupled to the HV Rectifier PC Board A12 by high voltage capacitor A12C7. A12CR2, A12CR3, A12C8, and A12R17 constitute a detector/voltage doubler circuit which converts the transfer oscillator output waveform into a negative dc signal which is coupled to A12-1 via A12R18. This signal has the same amplitude at A12-1 as the negative ac-coupled pulse applied to A12-1 via A12C6. Diode A12CR4 clamps the CRT grid to the (-) hv output line, permitting only negative-going signals to be coupled to the grid, as required to blank the trace. This prevents positive-going transients from causing bright spots at the start of each trace when the blanking signal is removed.

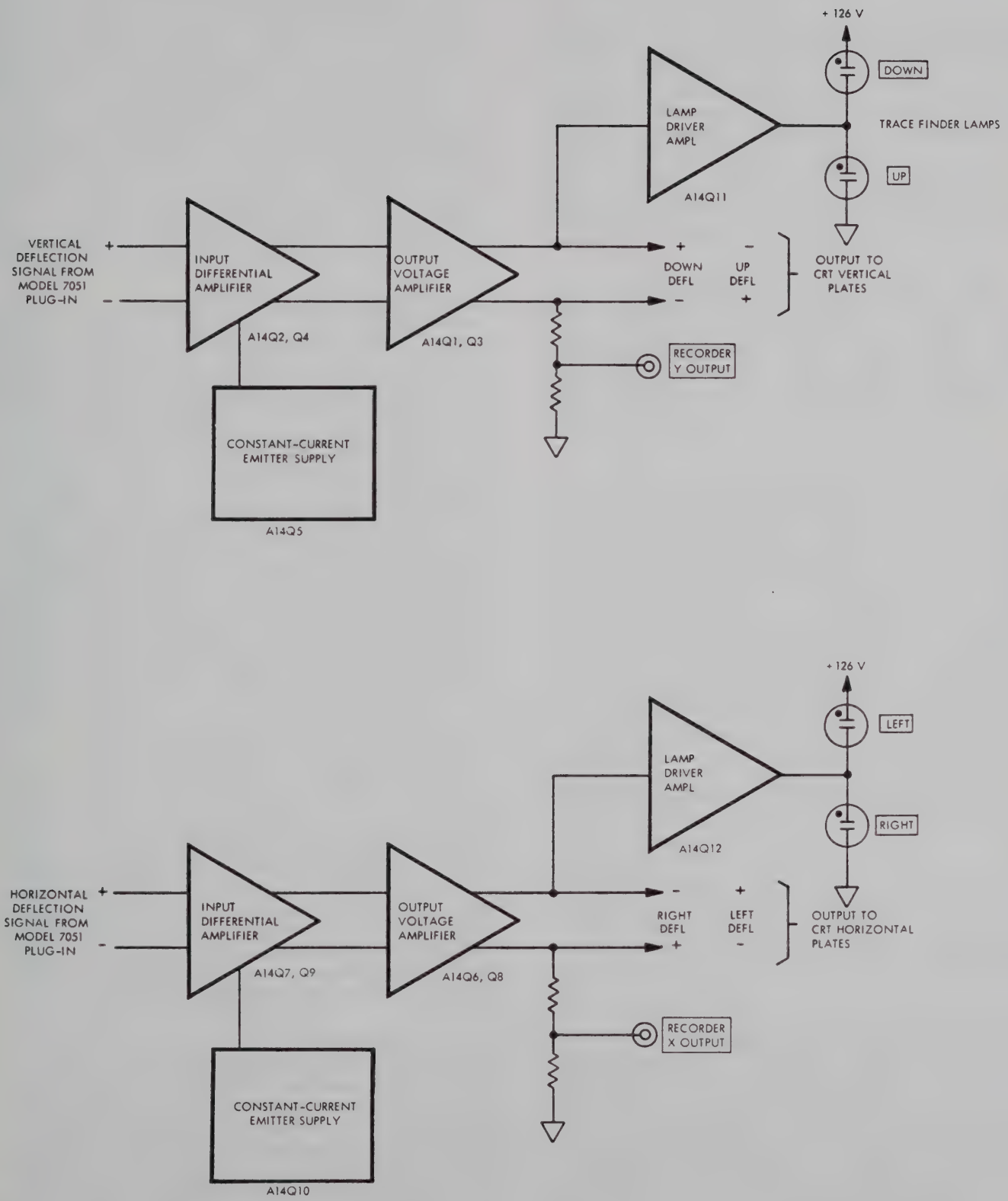


FIGURE 4-12. BLOCK DIAGRAM OF CRT DEFLECTION CIRCUITS (A14)

In summary, both blanking signals supplied by the plug-in circuit are positive-going when the CRT trace is to be blanked. The positive ac blanking signal, capacitively coupled directly to the cathode, cuts off the electron beam to blank the trace. The positive dc blanking signal, applied to A11Q5, increases the conduction of that transistor, thereby reducing the current through A11R12 and causing a negative-going pulse at the A11R12-A11Q5 collector junction. This negative pulse is capacitively coupled directly to the grid to cut off the electron beam and provide fast blanking response. The steady-state positive level during the blanking interval is amplified by A11Q6 and ac-converted by A11Q7, rectified and doubled by the doubler circuit in A12, and applied with negative polarity to the grid. When the dc blanking signal is removed from A11Q5, the positive-going pulse coupled to the grid circuits through A12C6 serves to discharge the doubler storage capacitor A12C8.

4.3.5 CRT DEFLECTION CIRCUITS. (See Figure 4-12 and Schematic 900806C). The horizontal and vertical deflection circuits, contained on CRT Deflection PC Board A14, are identical and have a rise time of less than 1 μs. The input signals for both vertical and horizontal drive are supplied by the plug-in unit. Each consists of a differential amplifier input stage (A14Q2/A14Q4 or A14Q7/A14Q9) driven by a constant-current emitter supply (A14Q5 or A14Q10) to enhance common-mode rejection, and an output differential voltage amplifier stage (A14Q1/A14Q3 or A14Q6/A14Q8). Each amplifier provides differential output of 0 to approximately ±60 V to move the CRT spot from center-scale to either extreme. The trace finder quadrant of neon indicator lights is driven by a pair of amplifiers (A14Q11 and A14Q12) which monitor the polarity of the differential output of each channel and control the corresponding pair of oppositely biased neon indicators to light one or the other as the trace moves on either side of center. The Recorder Drive Networks are fixed resistive networks which tap off a single-ended X-Y recorder output of about 0.2 V/cm from the differential deflection amplifier output stages.

4.3.5.1 Detailed Theory of CRT Deflection Circuits. Since the vertical and horizontal amplifier circuits are identical, only the vertical amplifier circuit will be described in detail. The differential input signal at A14-A and A14-P drives the bases of the input differential amplifier pair A14Q2 and A14Q4, which operate in the common-emitter configuration. Resistors A14R7 and A14R8, connected across the emitters of the differential pair, provide emitter degeneration for the amplifier. A14R8 adjusts the amount of degeneration and thereby sets the amplifier gain. A14R10 provides a balance adjustment to divide the emitter drive current from the constant-current emitter supply stage A14Q5 to provide equal response from the differential transistors so that 0 V differential output signal is supplied when the differential input signal is zero.

The constant-current emitter supply is temperature-compensated by A14CR1. A14R5 and A14R6, with A14CR1, provide a fixed base bias for A14Q5, and A14R12 establishes the low current generator source impedance. Constant-current operation is required to provide excellent common-mode rejection, so that the 0 V differential output condition between pins A14-C and A14-M occurs when both lines are at a voltage output equal to half the supply voltage, or approximately 63 V. Such common-mode rejection is important because the full peak-to-peak dynamic range of twice the supply voltage at the differential output cannot be obtained if the balanced output condition occurs at an offset voltage.

A14R3 and A14R2 load the differential amplifier base drive input circuit to prevent high frequency oscillations which might otherwise occur due to the resonant effects of the capacity of the shielded input leads.

The output differential voltage amplifier stage (A14Q1/A14Q3) operates in the common-base configuration, driven by A14Q2 and A14Q4 which essentially constitute a constant-current drive source. The output stage provides voltage gain without current gain. This mode permits safe operation of the 2N699 transistors with the collector at the full +126 V supply potential, a condition that could not be achieved with common-emitter operation. The load for A14Q1 and A14Q3 is provided by load resistors A14R1 and A14R13, and peaking coils A14L1 and A14L2. The peaking coils improve the amplifier bandwidth by compensating for the collector capacitance load.

4.3.5.2 Recorder Drive Signal Output. A14R35, A14R36, and A14R38 form a resistor network which brings out a single-ended recorder drive signal tapped from one-half of the differential output to the CRT. A14R38 also serves as the output source impedance. As the spot moves from the bottom to the top of the CRT, the output at A11-C varies from about 0 V to +126 V, and the single-ended output at A11-J changes from about 0 V to > +2 V.

4.3.5.3 Trace Finder Lamp Circuit. The other half of the differential output circuit is also tapped to drive a trace-position indicating circuit consisting of A14Q11, A14R42, R10, R11, DS6, and DS7. When the output signal drives the spot toward the bottom of the CRT, or off-screen in that direction, the voltage at pin A14-M will be > +70 V and A14Q11 will be biased to heavy conduction. This will drop pin A14-L (and one side of DS6, through R10) to ≈ 0 V. Since the +126 V supply is connected directly to the other side of DS6, the voltage drop will energize the DOWN lamp. When the output signal drives the spot toward the top of the CRT, or off-screen in that direction, the voltage at pin A14-M will be < +50 V, and the voltage-divider action of A14R32 and A14R43, returned to -12.6 V, will bias A14Q11 to cut off. With negligible current then being drawn through A14R42, the voltage at pin A14-L (and one side of DS7, through R11) will approach +126 V. Since the other side of DS7 is connected directly to ground, the voltage drop will energize the UP lamp.

The appropriate lamps thus are lit long before the trace goes off-screen, and with fast dual-trace presentations it is possible for all four lamps to be lit with an on-screen presentation. When the trace is "lost" off-screen, only the lamp in the appropriate direction will be lit, permitting instant locating of the trace.

4.3.5.4 Trace Alignment Adjustment Circuit. The TRACE ALIGNMENT control R7 applies an adjustable bias to alignment coil L1 which is wrapped around CRT inside the shield. This permits the operator to align the trace with the graticule. Since the CRT shield cannot provide 100% shielding against the earth's magnetic field and adjacent electronic instruments, this alignment coil is required to allow the operator to obtain perfect horizontal alignment of the presentation for any installation position. Because the pivot point of the alignment axis may not coincide with the CRT center, it is preferable to align the trace before calibrating test set-ups so that no shift in the calibration vertical intercept will occur.

SECTION 5

MAINTENANCE

5.1 PERIODIC MAINTENANCE.

Every few months perform the following maintenance on the Model 8000/7051.

a. Remove all accumulated dust with forced air.

b. Visually inspect the unit for loose or broken connections, loose panel controls or connectors, improperly seated PC Boards, etc. Make any indicated repairs or replacements.

c. Check supply voltages at test points as directed in Paragraph 5.2.

d. Make a performance test in accordance with the procedure of Paragraph 2.6.

NOTE: All required lubrication is performed at the factory during assembly. Additional lubrication should not be required in the field.

5.2 SUPPLY VOLTAGE MEASUREMENTS AT CHASSIS TEST POINTS.

Test points are provided on the Model 8000 chassis at the outputs of the low and high voltage supplies. These test points are located on the center bulkhead of the chassis, adjacent to the CRT shield, as shown in Figure 5-1. A check of those supply outputs should be made as the first step in a routine performance check or in locating the cause of malfunction. The low voltage supplies, listed in Table 5-1, should be checked first, since the high voltage supply and most other circuits of the instrument cannot operate properly with out-of-spec low voltages. The low voltage supplies are measured with respect to chassis ground (GND testpoint), and any accurate digital meter can be used.

Table 5-1. Supply Voltage Test Point Measurements

LOW VOLTAGE SUPPLY OUTPUTS
Measured with respect to Chassis Ground (TP6 GND) with Standard Digital Meter (Listed in preferred order of measurement)

Supply	TP#	DC Voltage & Tolerance	AC Ripple
-12.6 V	TP5	-12.6 ± 0.01 V dc	< 0.5 mv
+12.6 V	TP4	+12.6 ± 0.2 V dc	< 0.5 mv
+126 V	TP3	+126 ± 3 V dc	< 10 mv

HIGH VOLTAGE SUPPLY OUTPUT
Measured with Respect to Chassis Ground (TP6 GND) with High Voltage Digital Meter or Suitable Voltage-Divider Probe.

Supply	TP#	DC Voltage & Tolerance	AC Ripple
2.5 KV	TP7	-2.5 ± 0.1 KV	< 5 V

The high voltage supply (-2.5 KV) test point, listed in Table 5-1, is located next to the low voltage supply test points. This voltage is also measured with respect to chassis ground, and a high-voltage voltmeter or a digital meter with a high-voltage probe must be used.

5.3 INTERNAL ADJUSTMENTS

CAUTION

Before attempting to make ANY adjustments of chassis calibration controls, read all the material under this heading. Improper adjustments can degrade the accuracy of the instrument, and can require lengthy re-calibration procedures to restore proper performance.

5.3.1 AVAILABLE ADJUSTMENTS. There are 23 internal adjustments in the Model 8000/7051. The instrument is designed for long-term operation with a minimum of adjustment. The factory calibration is carefully performed so that specified accuracy is obtained throughout the 60 db dynamic operating range. The 23 adjustments include 19 "critical" adjustments which should not need field adjustment unless components are replaced in the critical circuits calibrated by these adjustments. The other 4 adjustments can be used for periodic recalibration at six-month intervals or as required. These two different classes of adjustments, and their uses, are described separately in Paragraphs 5.3.2 and 5.3.3.

5.3.2 CRITICAL ADJUSTMENTS. The critical adjustments must be adjusted using the specialized calibration techniques given in the detailed procedures of Paragraph 5.3.4, and following the sequence specified therein, working from the high-level CRT drive circuits back to the low-level input stage circuits. If not adjusted in accordance with the procedure of Paragraph 5.3.4, the critical adjustments can degrade factory calibration accuracy, and/or interact with other adjustments in a complex way to seriously degrade performance without permitting simple diagnosis of the mis-adjustment. These critical adjustments are located in stabilized circuits protected against in-service component variations. They should not require any further adjustment in the field unless damage or component failure occurs in the critical circuits calibrated by these adjustments. If calibration is required because of replacement of parts in a critical circuit, or because results of a signal tracing check are unsatisfactory, the optimum manner of performing the critical adjustments is given in Paragraph 5.3.4. The function of each adjustment is described briefly in the subparagraphs below. A factory calibration service is available at nominal cost by returning the instrument to ALFRED. Contact your nearest representative or our Sales Department.

a. A1R35 A CHN AMPL BAL ADJ. Provides a coarse balance adjustment for the base-emitter drop of each half of differential input amplifier stage Q1, to bring the operating conditions within the balancing range of the precision front panel A CHN BAL Screwdriver Control or the automatic balance circuit.

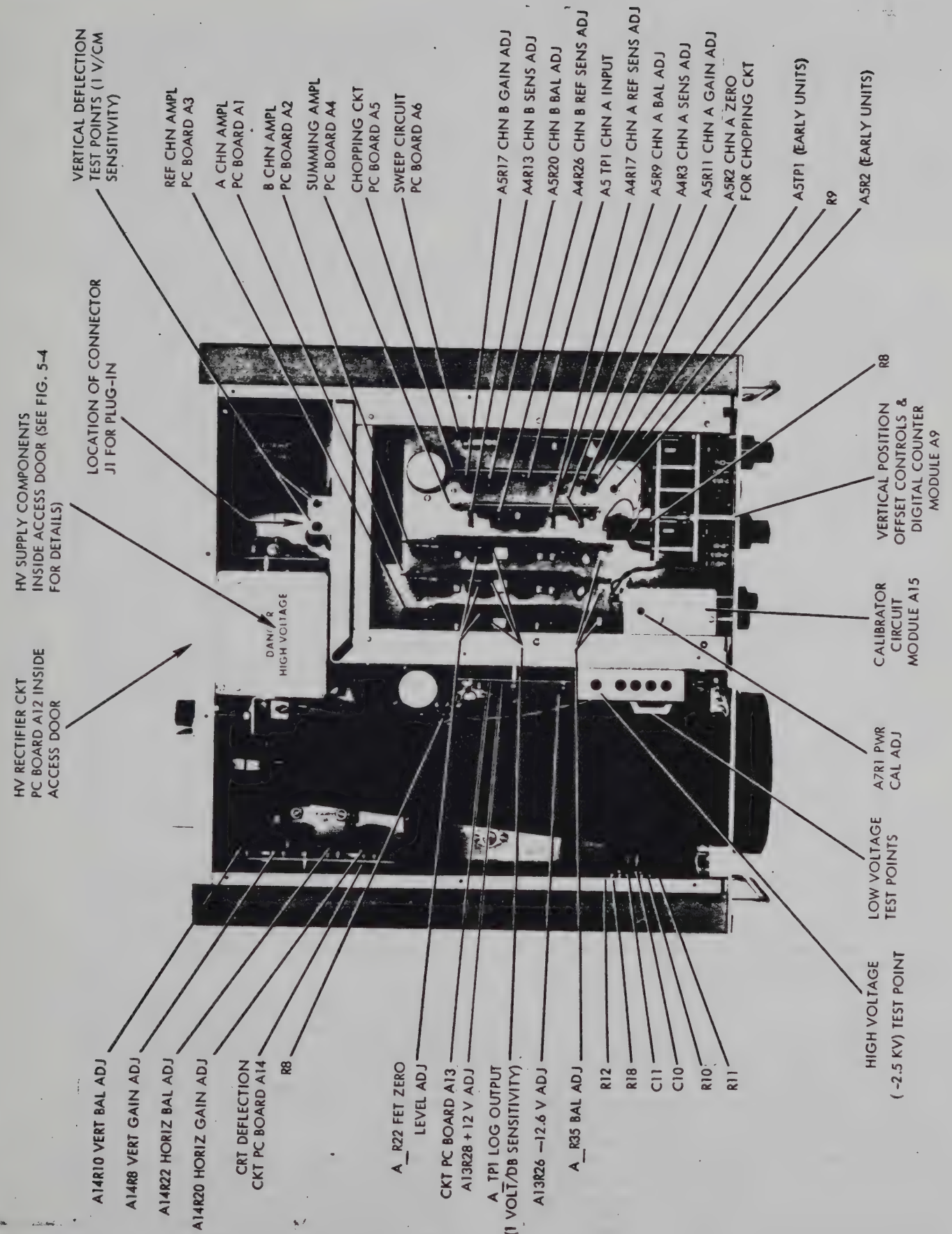

VERTICAL DEFLECTION TEST POINTS (1 V/CM SENSITIVITY)
REF CHN AMPL PC BOARD A3
A CHN AMPL PC BOARD A1
B CHN AMPL PC BOARD A2
SUMMING AMPL PC BOARD A4
CHOPPING CKT PC BOARD A5
SWEEP CIRCUIT PC BOARD A6
A5R17 CHN B GAIN ADJ
A4R13 CHN B SENS ADJ
A5R20 CHN B BAL ADJ
A4R26 CHN B REF SENS ADJ
A5 TP1 CHN A INPUT
A4R17 CHN A REF SENS ADJ
A5R9 CHN A BAL ADJ
A4R3 CHN A SENS ADJ
A5R11 CHN A GAIN ADJ
A5R2 CHN A ZERO FOR CHOPPING CKT
A5TP1 (EARLY UNITS)
R9
A5R2 (EARLY UNITS)
R8
VERTICAL POSITION OFFSET CONTROLS & DIGITAL COUNTER MODULE A9
CALIBRATOR CIRCUIT MODULE A15
A7R1 PWR CAL ADJ
LOW VOLTAGE TEST POINTS
HIGH VOLTAGE (-2.5 KV) TEST POINT
HV SUPPLY COMPONENTS INSIDE ACCESS DOOR (SEE FIG. 5-4 FOR DETAILS)
LOCATION OF CONNECTOR J1 FOR PLUG-IN
HV RECTIFIER CKT PC BOARD A12 INSIDE ACCESS DOOR
DANGER HIGH VOLTAGE
A14R10 VERT BAL ADJ
A14R8 VERT GAIN ADJ
A14R22 HORIZ BAL ADJ
A14R20 HORIZ GAIN ADJ
CRT DEFLECTION CKT PC BOARD A14
R8
A_R22 FET ZERO LEVEL ADJ
CKT PC BOARD A13
A13R28 +12 V ADJ
A_TP1 LOG OUTPUT (1 VOLT/DB SENSITIVITY)
A13R26 -12.6 V ADJ
A_R35 BAL ADJ
R12
R18
C11
C10
R10
R11

FIGURE 5-1. TOP VIEW OF MODEL 8000/7051

b. A1R22 A CHN AMPL FET ZERO ADJ. Compensates for gate-source drop in FET transistor A1Q8 to permit precise referencing of the A Channel automatic balance circuit to chassis ground.

c. A2R35 B CHN AMPL BAL ADJ. Provides a coarse balance adjustment for the base-emitter drop of each half of differential input amplifier stage Q2, to bring the operating conditions within the balancing range of the precision front panel B CHN BAL Screwdriver Control or the automatic balance circuit.

d. A2R22 B CHN AMPL FET ZERO ADJ. Compensates for gate-source drop in FET transistor A2Q8 to permit precise referencing of the B Channel automatic balance circuit to chassis ground.

e. A3R35 REF CHN AMPL BAL ADJ. Provides a coarse balance adjustment for the base-emitter drop of each half of differential input amplifier stage Q3, to bring the operating conditions within the balancing range of the front panel REF CHN BAL Screwdriver Control or the automatic balance circuit.

f. A3R22 REF CHN AMPL FET ZERO ADJ. Compensates for gate-source drop in FET transistor A3Q8 to permit precise referencing of the REF Channel automatic balance circuit to chassis ground.

g. A4R3 SUMMING AMPL CHN A SENS ADJ. Adjusts the impedance of the summing amplifier Channel A input circuit to the signal supplied by the A Channel Amplifier A1, in order to match the signal sensitivity in volts/db to the precision reference output of the A CHN VERTICAL POSITION Offset Control R8.

h. A4R13 SUMMING AMPL CHN B SENS ADJ. Adjusts the impedance of the summing amplifier Channel B input circuit to the signal supplied by the B Channel Amplifier A2, in order to match the signal sensitivity in volts/db to the precision reference output of the B CHN VERTICAL POSITION Offset Control R9.

i. A4R17 SUMMING AMPL CHN A REF SENS ADJ. Adjusts the impedance of the summing amplifier Channel A input circuit to the signal supplied by the REF Channel Amplifier A3, in order to match the signal sensitivity in volts/db to the precision reference output of the A CHN VERTICAL POSITION Offset Control R8.

j. A4R26 SUMMING AMPL CHN B REF SENS ADJ. Adjusts the impedance of the summing amplifier Channel B input circuit to the signal supplied by the REF Channel Amplifier A3, in order to match the signal sensitivity in volts/db to the precision reference output of the B CHN VERTICAL POSITION Offset Control R9.

k. A5R2 CHOPPING CKT CHN A ZERO ADJ. Adjusts the base bias of the chopping circuit Channel A differential amplifier input stage to establish precisely zero-level output under no-signal input conditions, to enhance the accuracy of this channel when used for high-sensitivity readout of input drift in A1, A2, or A3 for manual balancing operations.

l. A5R9 CHOPPING CKT CHN A BAL ADJ. Adjusts the relative emitter current distribution between transistors A5Q1 and A5Q2 of the chopping circuit Channel A differential amplifier to provide 0 V differential output when the signal input to both transistors is 0 V.

m. A5R11 CHOPPING CKT CHN A GAIN ADJ. Adjusts the gain of the chopping circuit Channel A differential amplifier to provide output sensitivity of exactly 1 V/cm, in response to the precision reference output of the A CHN VERTICAL POSITION Offset Control, R8, with a scale factor established by the A CHN VERTICAL SENSITIVITY control, S4.

n. A5R17 CHOPPING CKT CHN B GAIN ADJ. Adjusts the gain of the chopping circuit Channel B differential amplifier to provide output sensitivity of exactly 1 V/cm, in response to the precision reference output of the B CHN VERTICAL POSITION Offset Control, R9, with a scale factor established by the B CHN VERTICAL SENSITIVITY control, S5.

o. A5R20 CHOPPING CKT CHN B BAL ADJ. Adjusts the relative emitter current distribution between transistors A5Q4 and A5Q5 of the chopping circuit Channel B differential amplifier to provide 0 V differential output when the signal input to both transistors is 0 V.

p. A14R10 CRT DEFLECTION CKT VERT BAL ADJ. Adjusts the emitter-to-emitter resistance in transistors A14Q2 and A14Q4 of the differential input stage of the vertical deflection amplifier so that with the differential signal input terminals shorted, the CRT trace is centered vertically on the graticule.

q. A14R8 CRT DEFLECTION CKT VERT GAIN ADJ. Adjusts the gain of the differential input stage of the vertical deflection amplifier, so that a 1 V differential input signal produces a CRT deflection of exactly 1 cm.

r. A14R22 CRT DEFLECTION CKT HORIZ BAL ADJ. Adjusts the emitter-to-emitter resistance in transistors A14Q7 and A14Q9 of the differential input stage of the horizontal deflection amplifier, so that with the differential signal input terminals shorted, the CRT trace is centered horizontally on the graticule.

s. A14R20 CRT DEFLECTION CKT HORIZ GAIN ADJ. Adjusts the gain of the differential input stage of the horizontal deflection amplifier, so that a 1 V differential input signal produces a CRT deflection of exactly 1 cm.

5.3.3 PERIODIC RECALIBRATION ADJUSTMENTS. The following adjustments are denoted as "non-critical" because they can be set individually by observation or measurement, independently of the procedure of Paragraph 5.3.4, without interacting with other controls. They may be checked and field-set to perform periodic recalibration. They should also be used to calibrate performance after parts have been replaced in the associated supplies. The adjustments and recommended adjustment procedures, are given below:

a. A13R26 LV POWER SUPPLY -12.6 V ADJ (Fig. 5-1). This adjustment is used to set the -12.6 V supply output at TP5 to -12.60 V dc ± 0.01 V dc with respect

to chassis ground (GND TP6). Because the accuracy and stability of the supply circuits in the Model 8000 approach that of the best test equipment, only a 0.01% digital voltmeter that has recently been calibrated should be used to check this voltage. When the measured value falls anywhere within the tolerance range indicated, no adjustment should be performed. This adjustment should be checked after replacing regulator transistor Q3 on the Model 8000 chassis or regulator amplifier transistors A13Q8, A13Q9, or A13Q10 on the L V Power Supply PC Board A13. This adjustment serves as the master calibration adjustment for all the low voltage supplies, since they are all referenced to the -12.6 V supply.

b. A13R28 L V POWER SUPPLY +12.6 V ADJ (S/N 301 & up; Fig. 5-1). This adjustment is used to set the +12.6 V supply output at TP4 to +12.60 V dc ± 0.01 V dc with respect to chassis ground (GND TP6). Use a .01% digital voltmeter and do not make any adjustment unless the measured value falls outside the indicated tolerance range. This adjustment should be checked after replacing regulator transistor Q2 on the Model 8000 chassis or regulator amplifier transistors A13Q5, A13Q6, or A13Q7 on the L V Power Supply PC Board A13.

c. A12R2 INT. LIMIT ADJ. (Fig. 3-2). This adjustment is used to set the CRT trace intensity control range provided by the front panel TRACE INTENSITY control. To adjust A12R2, turn the front panel TRACE INTENSITY control fully CCW, and set A12R2 to the point where the trace is just extinguished. Note that use of excessively high intensity levels can burn the CRT screen phosphors and will shorten CRT life. This adjustment can be used to compensate for the gradual dropoff in trace intensity that occurs as the CRT ages. The adjustment should be checked whenever the CRT is replaced or after any component in the HV supply or High Voltage Rectifier PC Board A12 is replaced.

d. A12R4 FOCUS ADJ (Fig. 3-2). This adjustment is used to set the CRT trace sharpness (focus) to obtain the thinnest possible line at any desired level of brilliancy. To adjust A12R4, turn the front panel TRACE INTENSITY control to the desired intensity level, and set A12R4 to achieve the best focus. There is some interaction between these two controls, so the procedure may have to be repeated to achieve both optimum focus and the desired intensity.

e. A7R1 PWR CAL ADJ. This adjustment sets the oscillator signal amplitude in the RF Calibrator assembly so that the absolute output level provided at the OUTPUT CALIBRATOR jack tracks the CALIBRATOR switch settings. This adjustment should be checked whenever any component on Calibrator PC Board A7 is replaced, and at other times as desired to verify the absolute accuracy of the calibrator circuit for absolute level measurement calibration. Note that the relative accuracy of the attenuator network operated by the CALIBRATOR switch is independent of the oscillator amplitude adjustment, so that detector compensation calibration and ratio measurement zero-set calibration are essentially independent of the adjustment of A7R1. To adjust A7R1, set the CALIBRATOR switch at +10 DBM, and connect the OUTPUT CALIBRATOR jack to the detector of a power meter which is capable of reading +10 dbm. Assure that the Calibrator output is on with a full duty cycle by avoiding any horizontal sweep which would cause the Calibrator to be modulated "off" during retrace, thereby reducing the reading of a slow-response power meter (i.e. see that HORIZONTAL POSITION SENSITIVITY switch is out of the INTERNAL SWEEP position, and that no signal is connected to the INPUT HORIZONTAL jack). Place the DISPLAY Mode Selector switch in any RATIO or LOG position to disable the automatic internal sweep provided in all BAL or CAL modes.

5.3.4 PROCEDURE FOR PERFORMING CRITICAL ADJUSTMENTS.

CAUTION

Failure to follow the procedures specified can increase the calibration time many fold and/or degrade performance specifications. Before proceeding, read Paragraph 5.3.2, and check the - and + 12.6V supply outputs at TP5 and TP4, adjusting these supplies in accordance with Paragraphs 5.3.3 a and b if necessary.

a. With the POWER switch turned off, remove the Sweep Network Analyzer Plug-in.

b. Turn the POWER switch ON, and allow 5 minutes for the instrument temperature to stabilize.

c. Short the VERT. DEF. test points TP8 and TP9 (Fig. 5-1).

d. Short pins 7 and 19 of connector J1 for the Sweep Network Analyzer Plug-in (Fig. 5-1).

e. Carefully examine the spot on the CRT. It should be positioned exactly in the center of the CRT, at the intersection of the horizontal and vertical centerlines. If the spot is off-center horizontally, restore it to the proper position by adjusting A14R22. If it is off-center vertically, restore it to the proper position by adjusting A14R10.

f. Remove the shorts installed in steps c and d above.

g. Apply a voltage of 4.00 V from a dc source with floating output to the VERT. DEF. test points TP8 and TP9, with the polarity indicated.

h. The trace spot should move up exactly 4 cm on the graticule. If the spot is not coincident with the 4-cm line, above the centerline, adjust A14R8 to move it to that position.

i. Reverse the polarity of the voltage connected to the VERT. DEF. test points TP8 and TP9.

j. The trace spot should move down exactly 4 cm on the graticule. If the spot is not coincident with the 4-cm line below the centerline, adjust A14R8 to move it closer to that position.

k. If adjustment was required in both steps h and j or in step j above, repeat steps g through j and set A14R8 to equalize the slight error in each direction.

l. Apply a voltage of 4.00 V from a dc source with floating output to pins 7 and 19 of connector J1 for the Plug-in, with + output to pin 7 and - output to pin 19.

m. The trace spot should move to the right exactly 4 cm on the graticule. If the spot is not coincident with the 4-cm line to the right of the centerline, adjust A14R20 to move it to that position.

n. Reverse the polarity of the voltage connected to pins 7 and 19 of J1.

o. The trace spot should move to the left exactly 4 cm on the graticule. If the spot is not coincident with the 4-cm line to the left of the centerline, adjust A14R20 to move it closer to that position.

p. If adjustment was required in both steps m and o, or in step o alone, repeat steps l through o and set A14R20 to equalize the slight error in each direction.

q. Turn the POWER switch off. Then insert the Sweep Network Analyzer Plug-in. Do not connect any inputs to the three channel INPUTS jacks.

r. With the POWER still off, mark Channel Amplifier PC Boards A1, A2, and A3 with individual identification tapes and then remove all three boards.

s. Make the following control settings on the Model 7051:
DISPLAY Mode Selector to RATIO A ÷ REF
CALIBRATOR to OFF
VERTICAL SENSITIVITY to .5 DB/DIV (both channels)
HORIZONTAL POSITION to center the trace
HORIZONTAL SENSITIVITY to INTERNAL SWEEP

t. Turn the POWER switch ON.

u. Ground test point A5TP1 (Fig. 5-1).

v. The CRT trace should be coincident with the horizontal centerline of the graticule. If it is not, adjust A5R9 to restore the trace to the centered position.

NOTE: If the trace slopes from side to side, adjust the panel TRACE ALIGNMENT Screwdriver control to align the trace exactly in the horizontal plane.

w. Remove the ground connection from test point A5TP1, that was installed in step u above.

x. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to center the trace.

y. Switch the A CHN VERTICAL SENSITIVITY switch through its full range, and note the effect on the trace. If the trace moves as sensitivity is adjusted, make a slight additional adjustment of the red A CHN VERTICAL POSITION knob until the trace remains stationary when sensitivity is changed.

z. Adjust A5R2 to position the trace exactly on the horizontal centerline of the graticule.

aa. Set the DISPLAY Mode Selector to RATIO B ÷ REF

ab. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to center the trace.

ac. Switch the B CHN VERTICAL SENSITIVITY switch through its full range, and note the effect on the trace If the trace moves as sensitivity is adjusted, make a slight additional adjustment of the red B CHN VERTICAL POSITION knob until the trace remains stationary when sensitivity is changed.

ad. Adjust A5R20 to position the trace exactly on the horizontal centerline of the graticule.

ae. Connect a floating Digital Voltmeter with a range of 0 to ± 10 V to the VERT DEFL test points TP8 and TP9 (Fig. 5-1).

af. Set the B CHN VERTICAL SENSITIVITY switch to 0.5 DB/DIV.

ag. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to bring the DVM indication to 0.00 volts. (This should also center the trace on the CRT.) Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 0.00. Then turn the black knob fully CCW, out of the PRESET position.

ah. Set the B CHN VERTICAL SENSITIVITY switch to 10 DB/DIV.

ai. Turn the red B CHANNEL VERTICAL POSITION knob CW to achieve an offset of 50.0 LOSS DB as indicated on the digital counter.

aj. The voltage between TP8 and TP9, as indicated on the DVM, should be 5.00 ± 0.01 V (and the trace should be positioned 5 cm above the horizontal graticule centerline). If necessary, adjust A5R17 to obtain the above voltage on the DVM.

ak. Turn the red B CHANNEL VERTICAL POSITION knob CCW to achieve an offset of 50.0 GAIN DB as indicated on the digital counter.

al. The voltage between TP8 and TP9, as indicated on the DVM, should be -5.00 ±0.1 V (and the trace should be positioned 5 cm below the horizontal graticule centerline). If the voltage is incorrect, adjust A5R17 to eliminate half the error voltage. Then repeat steps ai and aj and re-adjust A5R17 slightly as necessary to equalize the errors in the two measurements. Recheck the B channel balance in accordance with steps ab through ad.

am. Repeat steps ai through al, without adjusting A5R17, to check the other sensitivity settings. Results should be as tabulated below. If necessary, make a slight re-adjustment of A5R17, to equalize the errors between all sensitivity settings.

B CHN VERTICAL SENSITIVITY	B CHANNEL VERTICAL POSITION	DVM INDICATION
5 DB/DIV	25.0 LOSS DB	5.00 ± 0.1 V
5 DB/DIV	25.0 GAIN DB	-5.00 ± 0.1 V
2 DB/DIV	10.0 LOSS DB	5.00 ± 0.1 V
2 DB/DIV	10.0 GAIN DB	-5.00 ± 0.1 V
1 DB/DIV	5.0 LOSS DB	5.00 ± 0.1 V
1 DB/DIV	5.0 GAIN DB	-5.00 ± 0.1 V
0.5 DB/DIV	2.5 LOSS DB	5.00 ± 0.1 V
0.5 DB/DIV	2.5 GAIN DB	-5.00 ± 0.1 V

an. Set the DISPLAY Mode Selector to Ratio A ÷ REF.

ao. Set the A CHN VERTICAL SENSITIVITY switch to 0.5 DB/DIV.

ap. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to bring DVM indication to 0.00 volts. (This should also center the trace on the CRT.) Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 0.00. Then turn the black knob fully CCW, out of the PRESET position.

aq. Set the A CHN VERTICAL SENSITIVITY switch to 10 DB/DIV.

ar. Turn the red A CHANNEL VERTICAL POSITION knob CW to achieve an offset of 50.0 LOSS DB as indicated on the digital counter.

as. The voltage between TP8 and TP9, as indicated on the DVM, should be 5.00 ± 0.01 V (and the trace should be positioned 5 cm above the horizontal graticule centerline). If necessary, adjust A5R11 to obtain the above voltage on the DVM.

at. Turn the red A CHANNEL VERTICAL POSITION knob CCW to achieve an offset of 50.0 GAIN DB as indicated on the digital counter.

au. The voltage between TP8 and TP9, as indicated on the DVM, should be -5.00 ±0.1 V (and the trace should be positioned 5 cm below the horizontal graticule centerline). If the voltage is incorrect, adjust A5R11 to eliminate half the error voltage. Then repeat steps ar and as and re-adjust A5R11 slightly as necessary to equalize the errors in the two measurements. Recheck the A channel balance in accordance with steps u through w.

av. Repeat steps ar through au, without adjusting A5R11, to check other sensitivity settings. Results should be as tabulated below. If necessary, make a slight re-adjustment of A5R11, to equalize the errors between all sensitivity settings.

A CHN VERTICAL SENSITIVITY	A CHANNEL VERTICAL POSITION	DVM INDICATION
5 DB/DIV	25.0 LOSS DB	5.00 ± 0.1 V
5 DB/DIV	25.0 GAIN DB	-5.00 ± 0.1 V
2 DB/DIV	10.0 LOSS DB	5.00 ± 0.1 V
2 DB/DIV	10.0 GAIN DB	-5.00 ± 0.1 V
1 DB/DIV	5.0 LOSS DB	5.00 ± 0.1 V
1 DB/DIV	5.0 GAIN DB	-5.00 ± 0.1 V
0.5 DB/DIV	2.5 LOSS DB	5.00 ± 0.1 V
0.5 DB/DIV	2.5 GAIN DB	-5.00 ± 0.1 V

aw. Disconnect the DVM from VERT. DEF. test points TP8 and TP9.

ax. Turn the Model 8000 POWER switch off.

ay. Replace the Channel Amplifier PC Boards A1, A2, and A3 that were removed in step r above.

az. Turn the POWER switch ON.

ba. Set the DISPLAY Mode Selector switch to BAL A CHN.

bb. Connect a short (or detector) across the A CHN INPUT connector.

bc. Turn the front panel A CHN BALANCE Screwdriver control to its mechanical center.

bd. Adjust R35 on board A1 to position the trace as close as possible to the CRT centerline.

be. Adjust the front panel A CHN BALANCE Screwdriver control to position the trace exactly on the CRT centerline.

bf. Set the DISPLAY Mode Selector switch to BAL REF CHN.

bg. Connect a short (or detector) across the REF CHN INPUT connector.

bh. Turn the front panel REF CHN BALANCE Screwdriver control to its mechanical center.

bi. Adjust R35 on board A3 to position the trace as close as possible to the CRT centerline.

bj. Adjust the front panel REF CHN BALANCE Screwdriver control to position the trace exactly on the CRT centerline.

bk. Set the DISPLAY Mode Selector switch to BAL B CHN.

bl. Connect a short (or detector) across the B CHN INPUT connector.

bm. Turn the front panel B CHN BALANCE Screwdriver control to its mechanical center.

bn. Adjust R35 on board A2 to position the trace as close as possible to the CRT centerline.

bo. Adjust the front panel B CHN BALANCE Screwdriver control to position the trace exactly on the CRT centerline.

bp. Remove the short-circuit from the three Channel INPUTS connectors if shorts were used.

bq. Set all three +10 CAL Screwdriver controls on the front panel to their mechanical centers.

br. Connect crystal detectors (ALFRED Model 1001 or equivalent) to the three Channel INPUTS connectors.

bs. Make the following front panel settings:

DISPLAY Mode Selector to CAL A CHN
DISPLAY BALANCE Switch to AUTO
CALIBRATOR Switch to -20 DBM
VERTICAL SENSITIVITY to 0.5 DB/DIV (both channels)

bt. Connect the rf input port of the Channel A crystal detector to the OUTPUT CALIBRATOR jack.

bu. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to exactly center the trace. Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position.

bv. Turn the CALIBRATOR switch to +10 DBM and adjust the red A CHANNEL VERTICAL POSITION knob to set the digital counters to 30.0 GAIN DB.

bw. The trace should still be positioned exactly on the CRT horizontal centerline. If not, note the amount by which the trace is displaced from the centerline, and adjust the A CHN +10 CAL panel screwdriver adjustment to position the trace the same distance in the opposite direction from the centerline.

bx. Turn the CALIBRATOR switch to -20 DBM.

by. Repeat steps bu through bx until the trace is centered on the graticule without any adjustment being required in steps bu and bw.

bz. Turn the CALIBRATOR switch to -30 DBM and adjust the red A CHANNEL VERTICAL POSITION knob to set the digital counters to 10.0 LOSS DB.

ca. The trace should still be positioned exactly on the CRT horizontal centerline. If not, make an adjustment of A4R3. Note that the presentation does not indicate directly how far or in what direction to adjust A4R3. Therefore, it will be necessary to switch the CALIBRATOR between -30 DBM and -20 DBM and try several tentative adjustments of A4R3 until the setting is found which provides a 10 db change in display indication in response to the calibrator level change between -30 DBM and -20 DBM. Use the red A CHANNEL VERTICAL POSITION knob to return the trace to the centerline in each case, and monitor the deflection in db from the digital counter.

cb. Turn the CALIBRATOR switch to -20 DBM.

cc. If an adjustment of A4R3 was required in step ca, repeat steps bu through cb until no adjustments are required to obtain calibrated readout.

cd. Disconnect the Channel A crystal detector from the OUTPUT CALIBRATOR jack, and connect the rf input port of the Channel B crystal detector to the OUTPUT CALIBRATOR jack.

ce. Set the DISPLAY Mode Selector switch to CAL B CHN, and set the CALIBRATOR switch to -20 DBM.

cf. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to exactly center the trace. Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position.

cg. Turn the CALIBRATOR switch to +10 DBM and adjust the red B CHANNEL VERTICAL POSITION knob to set the digital counters to 30.0 GAIN DB.

ch. The trace should still be positioned exactly on the CRT horizontal centerline. If not, note the amount by which the trace is displaced from the centerline, and adjust the B CHN +10 CAL panel screwdriver adjustment to position the trace the same distance in the opposite direction from the centerline.

ci. Turn the CALIBRATOR switch to -20 DBM.

cj. Repeat steps cf through ci until the trace is centered on the graticule without any adjustment being required in steps cf and ch.

ck. Turn the CALIBRATOR switch to -30 DBM and adjust the red B CHANNEL VERTICAL POSITION knob to set the digital counters to 10.0 LOSS DB.

cl. The trace should still be positioned exactly on the CRT horizontal centerline. If not, make an adjustment of A4R13. Note that the presentation does not indicate directly how far or in what direction to adjust A4R13. Therefore, it will be necessary to switch the CALIBRATOR between -30 DBM and -20 DBM and try several tentative adjustments of A4R13 until the setting is found which provides a 10 db change in the display indication in response to the calibrator level change between -30 DBM and -20 DBM. Use the red B CHANNEL VERTICAL POSITION knob to return the trace to the centerline in each case, and monitor the deflection in db from the digital counter.

cm. Turn the CALIBRATOR switch to -20 DBM.

cn. If an adjustment of A4R13 was required in step cl, repeat steps cf through cm until no adjustments are required to obtain calibrated readout.

co. Disconnect the Channel B crystal detector from the OUTPUT CALIBRATOR jack, and connect the rf input port of the Channel REF crystal detector to the OUTPUT CALIBRATOR jack.

cp. Set the DISPLAY Mode Selector switch to CAL REF CHN and set the CALIBRATOR switch to -20 DBM.

cq. With the black A CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to exactly center the trace. Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position.

cr. Turn the CALIBRATOR switch to +10 DBM and adjust the red A CHANNEL VERTICAL POSITION knob to set the digital counters to 30.0 LOSS DB.

cs. The trace should still be positioned exactly on the CRT horizontal centerline. If not, note the amount by which the trace is displaced from the centerline, and adjust the REF CHN +10 CAL panel screwdriver adjustment to position the trace the same distance in the opposite direction from the centerline.

ct. Turn the CALIBRATOR switch to -20 DBM.

cu. Repeat steps cq through ct. until the trace is centered on the graticule without any adjustment being required in steps cq and cs.

cv. Turn the CALIBRATOR switch to -30 DBM and adjust the red A CHANNEL VERTICAL POSITION knob to set the digital counters to 10.0 GAIN DB.

cw. The trace should still be positioned exactly on the CRT horizontal centerline. If not, make an adjustment of A4R17. Note that the presentation does not indicate directly how far or in what direction to adjust A4R17. Therefore, it will be necessary to switch the CALIBRATOR between -30 DBM and -20 DBM and try several tentative adjustments of A4R17 until the setting is found which provides a 10 db change in the display indication in response to the calibration level change between -30 DBM and -20 DBM. Use the red A CHANNEL VERTICAL position knob to return the trace to the centerline in each case, and monitor the deflection in db from the digital counter.

cx. Turn the CALIBRATOR switch to -20 DBM.

cy. If an adjustment of A4R17 was required in step cw, repeat steps cq through cx until no adjustments are required to obtain calibrated readout.

cz. Leave the Channel REF crystal detector connected to the OUTPUT CALIBRATOR jack. Install a short on the CHN B INPUT jack.

da. Set the DISPLAY Mode Selector switch to RATIO B ÷ REF, and set the CALIBRATOR switch to -30 DBM.

db. With the black B CHANNEL VERTICAL POSITION knob turned fully CCW, out of the PRESET position, turn the red knob to exactly center the trace. Then turn the black knob to the PRESET position and use the red knob to set the digital counters to 00.0. Then turn the black knob fully CCW, out of the PRESET position.

dc. Turn the CALIBRATOR switch to -20 DBM and adjust the red B CHANNEL VERTICAL POSITION knob to set the digital counters to 10.0 LOSS DB.

dd. The trace should still be positioned exactly on the CRT horizontal centerline. If not, make an adjustment of A4R26. Note that the presentation does not indicate directly how far or in what direction to adjust A4R26. Therefore, it will be necessary to switch the CALIBRATOR between -30 DBM and -20 DBM and try several tentative adjustments of A4R26 until the setting is found which provides a 10 DB change in the display indication in response to the calibrator level change between -30 DBM and -20 DBM. Use the red B CHANNEL VERTICAL POSITION knob to return the trace to the centerline in each case, and monitor the deflection in db from the digital counter.

NOTE: Since the REF Channel input in this step is the denominator of the ratio measurement, the -20 DBM input will reduce the ratio (compared to the -30 DBM level) and will require LOSS DB offset to restore the trace to the CRT centerline when the digital counters have been set to 00.0 with a -30 DBM input level.

de. Monitor the automatic rebalance level of the Channel A Amplifier PC Board A1, at A1TP1, under the conditions listed in Figure 5-6. With a crystal detector connected to the A CHN INPUT jack, and with no input signal applied to the detector, the observed waveform should be similar to #13 of Figure 5-6. Adjust A1R22 to set the automatic rebalance level at exactly 0 V.

df. Monitor the automatic rebalance level of the Channel B Amplifier PC Board A2, at A2TP1, under the conditions listed in Figure 5-6. With a crystal detector connected to the B CHN INPUT jack, and with no input signal applied to the detector, the observed waveform should be similar to #13 of Figure 5-6. Adjust A2R22 to set the automatic rebalance level at exactly 0 V.

dg. Monitor the automatic rebalance level of the Channel REF Amplifier PC Board A3, at A3TP1, under the conditions listed in Figure 5-6. With a crystal detector connected to the REF CHN INPUT jack, and with no input signal applied to the detector, the observed waveform should be similar to #13 of Figure 5-6. Adjust A3R22 to set the automatic rebalance level at exactly 0 V.

5.4 TROUBLE SHOOTING

5.4.1 STEPS TO FOLLOW WHEN FAILURE OCCURS. First check all supply voltages in accordance with Paragraph 5.2 to help localize the trouble to a supply or other circuit. If none of the supplies provides an output, check fuse F1 on the rear panel. If some, but not all, supply outputs are satisfactory, turn power off and remove the Model 7051 plug-in. If no improvement is observed in the supply outputs when power is restored, the failure is probably a defective LV Power Supply Circuit A13 or a defective using circuit in the Model 8000; if supply performance is improved with the 7051 removed, check for shorted components in the plug-in unit. If all supply outputs are satisfactory, use the generalized procedure tabulated in Table 5-2 to localize the trouble to an individual chassis, PC board, or module. Use Table 5-3, when applicable, to locate and correct specific failures and faults. When the failure experienced is covered in Table 5-3, it should not be necessary to carry out the localization procedure of Table 5-2.

CAUTION

REMOVAL OF PC BOARDS. When a PC board extender is used for convenient access to one of the plug-in PC boards on the Model 7051 to allow making test measurements, or if a PC board is removed for component checking, observe the following precautions:

a. Always turn the POWER switch OFF before disconnecting or connecting any PC board, either directly to its receptacle or through the board extender. If this is not done, there is the possibility that some transistors will be burned out by transients that take place when the connection is made or broken.

b. While the board extender may be turned 180° as necessary to fit the keyed receptacles, the PC board being extended must always be kept in its normal orientation (see Fig. 5-1). If the PC board is inadvertently turned 180° extensive circuit damage may occur because of improper connections.

Table 5-2. Trouble Localization Chart

STEP	ACTION	INDICATION	POSSIBLE CAUSE OF TROUBLE
1.	With power off, remove Model 7051.	When power is restored, a centered spot should appear on the CRT.	If no spot appears check HV Supply and HV regulator and Blanking Circuits A11 and A12 using a high-voltage voltmeter or probe. Also check CRT. If an off-center spot occurs, check the calibration of CRT Deflection Circuit A14 in accordance with Paragraph 5.3.4.
2.	Connect a floating 5 V signal to the VERT DEF test points TP8 and TP9, with + to TP8.	Spot should move upward 5 cm on graticule.	If spot moves incorrectly, check the calibration of CRT Deflection Circuit A14 in accordance with Paragraph 5.3.4. If spot does not move, check components on CRT Deflection Circuit A14.
3.	Remove the test voltage connected in (2), and connect the floating 5 V signal to terminals 7 and 19 of plug-in connector J1, with + to #7.	Spot should move 5 cm to the right on graticule.	If spot moves incorrectly, check the calibration of CRT Deflection Circuit A14 in accordance with Paragraph 5.3.4. If spot does not move, check components on CRT Deflection Circuit A14.
4.	With power off install Model 7051. Then make waveform measurements in Sweep Circuit PC Board A6 under the operating conditions listed in Fig. 5-6, at the test points indicated in items 1 thru 7 of Fig. 5-6.	Waveforms should appear approximately as shown in Fig. 5-6.	If improper waveforms are observed, check the transistor concerned and associated components.
5.	Make waveform measurements in Chopping Circuit PC Board A5 under the operating conditions listed in Fig. 5-6, at the test points indicated in items 8 thru 12 of Fig. 5-6.	Waveforms should appear approximately as shown in Fig. 5-6.	If improper waveforms are observed, check the transistor concerned and associated components. Also check calibration in accordance with Paragraph 5.3.4
6.	With the DISPLAY MODE Selector in the LOG A CHN & B CHN position and with no input signals applied, set both VERTICAL SENSITIVITY Switches to 0.5 DB/DIV. Then move both traces to the CRT centerline by adjusting the VERTICAL POSITION controls. Make a further adjustment of exactly 2.5 db GAIN offset to move each trace to the bottom horizontal line of the graticule. Then adjust the VERTICAL SENSITIVITY controls through all positions and note the amount of VERTICAL POSITION offset adjustment required to restore the trace to the bottom graticule line.	Offset in db from the reading which places the trace on the graticule centerline should be as follows: VERTICAL SENSITIVITY Control Setting — GAIN OFFSET required to place trace on bottom graticule line 0.5 DB/DIV — 2.5 db 1 DB/DIV — 5 db 2 DB/DIV — 10 db 5 DB/DIV — 25 db 10 DB/DIV — 50 db NOTE: If the gain of either summing amplifier channel is apparently incorrect, it can be checked by measuring the voltage output/input ratio between terminals N and B (A Channel) or terminals T and Y (B Channel). The gain is controlled by the feedback supplied by the VERTICAL SENSITIVITY Switches, and with no other signals applied, it should be related to VERTICAL SENSITIVITY Switch settings approximately as follows: SENSITIVITY Switch Setting — Approximate Voltage Output/Input Ratio 0.5 DB/DIV — 2.5 1 DB/DIV — 1.25 2 DB/DIV — 0.63 5 DB/DIV — 0.25 10 DB/DIV — 0.13	If improper response is obtained, check calibration in accordance with Paragraph 5.3.4. If calibration cannot be set properly, check the components of A4.

Table 5-2. Trouble Localization Chart (Cont.)

STEP	ACTION	INDICATION	POSSIBLE CAUSE OF TROUBLE
7.	Move both traces to the CRT centerline by adjusting the VERTICAL POSITION controls. Then apply a -1 V signal from a 1 K source to the INPUT MARKERS jack under the operating conditions established in step 6 above.	The traces should move up approximately 1 - 2 cm when both VERTICAL SENSITIVITY Switches are set to 1 DB/DIV.	If improper response is obtained, check A4CR1, A4Q2, A4Q3 and associated components on PC Board A4.
8.	Make waveform measurements at TP1 in each Channel Amplifier PC Board (A1, A2, and A3) under the operating conditions listed in Fig. 5-6, at the test points indicated in items 13 and 14 of Fig. 5-6.	Waveforms should appear approximately as shown in Fig. 5-6. If CALIBRATOR is switched to higher power levels within the crystal square-law range (up to -20 DBM), the output level in Fig. 5-6 #14 should linearly track the power change. NOTE: The voltage output at TP1 vs the detector input power level supplied by the calibrator should have a sensitivity of 6 mv/db within the crystal square-law range and 3 mv/db within the linear range above the transition region.	If improper automatic rebalance response is obtained, check the rebalance circuit components (CR1, Q7, K1 and Q8) in the defective Channel Amplifier PC Board (A1, A2, or A3). If the amplifier does not linearly track power level changes < -20 DBM, check the logarithmic amplifier components including Q1, Q3 or Q5 and Q2, Q4, or Q6 in the oven Module A8 (corresponding to the defective Channel), and Q1 through Q6 on Channel Amplifier PC Board A1, A2, or A3.
9.	Check that OVEN TEMP STABILIZED light comes on after the instrument has been turned on for several minutes. If lamp does not turn on, monitor the collector current of oven heater transistor Q7 by one of two methods: (1) Connect a clip-on milliameter to the orange lead which drives the collector (Fig. 5-3) or (2) Remove fuse F1 (Fig. 5-3) and connect an ammeter across its terminals.	Current should be 1-2 amps at initial turn-on when the instrument is cold, dropping to 0 as proper oven temperature is reached, and then building up to a steady value of about 70 ma (50-100 ma depending upon ambient temperature) after 5-7 minutes to maintain the oven temperature. The OVEN TEMP STABILIZED light should come on at that time.	If current is improper, check the heater circuit including Q7 and RT1 and RT2 on Oven Assembly Module A8 and the circuits of A6Q9 thru A6Q11 on Sweep Circuit PC Board A6. If current is proper but light does not operate, check A6Q13 for open-circuit failure. Also check DS1 and the circuit of A6Q12.
10.	Check detector compensation calibration of each channel in accordance with Paragraph 3.5.	With proper compensation adjustment, readout of each level should track CALIBRATOR setting within ± 0.7 dbm.	If crystal cannot be properly compensated, check feedback transistors Q2, Q4 or Q6 in A8 (corresponding to the defective channel), and the compensation amplifier circuit including Q9, Q10, Q11, and CR3 thru CR7 on Channel Amplifier PC Board A1, A2 or A3.

Table 5-3. Trouble Shooting the Model 8000/7051

Trouble Indication	Suggested Cause and Remedy
1. Unable to manually balance a Channel using the front panel BALANCE screwdriver control for that Channel.	a. Internal BAL ADJ control A1R35* (Figure 5-1) for the defective Channel Amplifier PC Board A1/A2/A3 is improperly set so that front panel control does not operate within the range that achieves balance. Correct by first setting the front panel BALANCE control to mid-range, and then making the balance adjustment with the internal BAL ADJ control, A1R35*. Make a final vernier touch-up adjustment with the front panel control if necessary. b. If internal BAL ADJ control cannot be adjusted to achieve balance, return that control to its approximate initial position. Then interchange the Channel Amplifier PC Board A1/A2/A3 in the defective channel with one of the other two Channel Amplifier PC Boards in an operable channel. If the PC board from the defective channel balances satisfactorily in the other channel, the failure is in the input differential amplifier stage A8Q1/Q3/Q5 of the defective channel, and the oven-mounted differential transistor probably needs replacement. If the PC board from the defective channel is still inoperative when used in the other channel, the failure is in the PC board itself, and is probably due to failure or marginal performance from transistors A1Q1 and A1Q2 in the input differential amplifier stage*. Check the suspected transistors by substitution, and replace other components as necessary. NOTE: Be sure to replace the Channel Amplifier PC Boards into the channels in which they were originally operated. For trouble localization purposes, it is permissible to substitute an A1/A2/A3 board into another channel, but if each board is not returned to its original position, over-all calibration will be degraded, and each channel would have to be re-calibrated in accordance with Paragraph 5.3.4 to restore performance of the instrument.
2. Inadequate "hold" in automatic balance mode at -40 dbm operating level. (Inadequate "hold" means that the "automatic rebalance level" segment of the TP1 output waveform, as shown in #13 and 14 of Figure 5-6, jitters or charges to some level other than 0 V instead of being clamped to the 0 V ref. level during the interval between "output response level" segments of the trace.)	a. If the trouble is experienced only on one channel, check for marginal or inoperative components in the automatic rebalance circuit of the Channel Amplifier PC Board A1/A2/A3 in the defective channel. First check for excessive dirt and/or moisture build-up on the board, which can allow leakage in the gate drive circuit of FET transistor A1Q8. Clean the board as necessary with a non-residue type cleaner, and protect the job with a high-resistance overspray. If dirt is not the cause, check for failure in relay A1K1, and for excess leakage or failure in A1Q8 and/or A1C9*. b. If the trouble is experienced on all three channels, check for marginal or defective components in the circuit on Sweep PC Board A6 which generates the automatic rebalance control signal. (See item 3 below for details).
3. Inadequate "hold" in automatic balance mode at +20 dbm operating level. (Inadequate "hold" is defined in step #2 above; at +20 dbm it appears as improper clamping so that the output charges to some level other than 0 V during the automatic rebalance interval.)	a. If the trouble is experienced only on one channel, it is probably due to slow response from the Channel Amplifier PC Board A1/A2/A3 in the defective channel. This slow response can be caused by inadequate gain due to deterioration in performance of any transistor(s) in the logarithmic amplifier circuit on the board (A1Q1 - A1Q6). Replace the transistors in one differential stage at a time, working back from the output (A1Q5, A1Q6) to the input stage (A1Q1, A1Q2) until the trouble is eliminated.* b. If the trouble is experienced on all three channels, check for marginal or defective components in the circuit on Sweep PC Board A6 which generates the automatic rebalance control signal. Low gain in the A6Q7/A6Q14 stage can reduce the duration of the automatic rebalance control signal to less than 0.75 millisecond, which results in insufficient closure time for rebalance relay A1K1 in the Channel Amplifier PC Board. If the rebalance control signal duration (pulse width) is less than 0.75 millisecond, replace A6Q7 (and A6Q14 as applicable) with a higher $-\beta$ transistor to minimize the current drain on A6C5 and thereby increase the rebalance signal duration. Also check for excess leakage or failure in A6C5. (On units having the two-transistor Darlington stage with A6Q7 and A6Q14, a rebalance pulse duration of >1.25 milliseconds should be achieved.)

* Components listed for PC Board A1 apply to whichever Channel Amplifier PC Board is defective: A1, A2, or A3.

Table 5-3. Trouble Shooting the Model 8000/7051 (cont.)

Trouble Indication	Suggested Cause and Remedy
4. Erratic behavior when attempting to display low level signals with manual balancing, but proper operation is obtained with automatic rebalancing. (e.g. after obtaining proper no-signal manual balance trace in BAL mode, no response is obtained with -40 dbm input signal in LOG or RATIO modes; trace "suddenly" responds when signal level is raised to > -30 dbm, and then will "track" back to -40 dbm.)	Erratic failure of the logging transistor (A8Q2/Q4/Q6) in the inoperative channel. Replace the logging transistor and check the performance of the new transistor to assure that it does not exhibit the same behavior.
5. DC blanking signal is inoperative (i.e., CRT trace is not blanked during sweep retrace). NOTE: No harm is done in continuing to operate the instrument with this malfunction. Also, a small "tail" on the retrace in fast sweeps is normal.	Defective (shorted) A12CR4, due to application of an undesired transient between -2500 V and ground. Replace A12CR4. CAUTION: To avoid transients which can damage A12CR4, make all voltage and waveform measurements in high voltage circuits by turning power off before connecting or disconnecting the measurement instrument at each measurement point.
6. No CRT trace is visible. CAUTION: When making voltage measurements in high voltage circuits, turn power off before connecting or disconnecting the measurement instrument at each measurement point.	Localize to CRT, HV supply, or some other circuit by measuring the high voltage supply output voltage at TP7, and, if necessary, the electrode voltages on the CRT. With proper voltages applied, lack of a trace indicates a defective CRT which must be replaced. Improper HV supply output voltage indicates a defect in the supply oscillator, rectifier, or regulator circuits (see step 7 below). Improper anode voltages indicates failure in the bias networks supplying those voltages. Non-zero deflection plate voltages in the absence of applied signals indicates a malfunction in the signal amplifier circuitry which can be localized to the CRT Deflection PC Board A14, or to one of the PC Boards in the plug-in unit by circuit-tracing back from the deflection plates.
7. No output or improper output from HV supply. (see Caution in step 6.)	Measure output voltage at TP7, and follow the procedure below which corresponds to the voltage measured. a. If output voltage is 0 V, failure may be either in oscillator stage Q4 or in the regulator circuit of HV Regulator & Blanking PC Board A11. Localize by measuring the output voltage at A11-R. This voltage should be ≈ 0 V when no high voltage output is supplied, indicating that the regulator is attempting to draw more bias current through R6. 1. If the A11-R voltage is more than several volts below ground, the trouble is in the regulator circuit (A11Q1-A11Q4). Check each of these transistors and replace as necessary. Also check other components in the defective stage and replace as necessary. 2. If the A11-R voltage ≈ 0 V, the trouble is probably in oscillator transistor Q4. To check whether Q4 is shorted, turn power off and remove the high voltage supply access door (Figure 5-1). Then gently touch the Q4 can. If it is too hot to touch comfortably, it has shorted and has been drawing excess current. Replace Q4 and check other components in the oscillator stage. If Q4 feels only warm to the touch, it may be operating properly. Check the input and output voltages on T2, using a 10:1 divider probe and turning power off before connecting or disconnecting the probe at each measurement point. If input voltages are correct and output voltage is not ≈ 2.5 KV, check rectifier and filter components on HV Rectifier PC Board A12, and replace as necessary. If no oscillations appear on the input, check Q4 and associated components. b. If output voltage is not 0 V, but is low (-50 V to several hundred volts): 1. Check for defective components in the rectifier circuit of the HV Rectifier PC Board A12 (A12CR1, A12CR2, A12C1, A12C2, A12C3). Replace as necessary. 2. Check for defective components in the regulator circuit of HV Regulator and Blanking PC Board A11 or in the oscillator circuit (Q4), and replace as necessary. (See step a above.) c. If output voltage is high (> > 2.5 KV), check for defective components in the regulator circuit of HV Regulator and Blanking PC Board A11 (A11Q1 - A11Q4). If the regulator is working properly, the output at A11-R will be driven toward -12 V when the output voltage is too high, in response to heavy feedback current at A11-N. Also check for open resistors in the resistor dropping network on HV Rectifier PC Board A12 (A12R10 - A12R14), which supplies the feedback signal to the regulator. Replace defective components as necessary.

5.4.2 VOLTAGE AND WAVEFORM MEASUREMENTS. DC supply voltages are indicated on the schematics in Section 7. Waveform diagrams for those circuits where performance can best be monitored by oscilloscope are given in Fig. 5-6. Conditions of measurement are also given in the illustration. Keep in mind that the waveform measurements shown are typical, intended for use in localizing trouble in faulty circuits. In checking voltages, keep in mind that normal component variations can produce voltage variations commensurate with the component tolerances used in any particular circuit.

CAUTION

All measurements should be made with respect to chassis ground, unless otherwise indicated.

Excercise extreme caution when checking high voltage circuits. Turn power off before connecting or disconnecting the measurement instrument (probe) at each measurement point, to avoid causing circuit-damaging transients.

5.4.3 LOCALIZATION OF TROUBLE TO INDIVIDUAL COMPONENTS. In addition to making voltage and waveform measurements, it may be necessary to perform some active or passive circuit testing to pinpoint the defective component(s). In most cases, the performance of a particular transistor that is forward-biased can be evaluated by shorting the emitter and base lead where circuit voltages permit, or by opening the base lead. In either case, the transistor will be turned off unless it is shorted. Resultant changes in circuit voltages can be monitored to determine whether the transistor is performing. If a transistor does not conduct when its V_{be} exceeds turn-on - as can be determined by in-circuit measurements of its lead voltages (this may require base-emitter shorting or base opening on other transistors to establish proper conditions) - it can be assumed to be open.

NOTE: The tab on all single transistors identifies the emitter lead. The tab on all dual transistors identifies the collector leads. The tab on FET's identifies the drain lead, and the Q8 terminals on the A1/A2/A3 PC boards are labeled S, G, and D to identify source, gate, and drain. On transistors with solid epoxy cases having no tab, the leads are arranged in a standard semicircle with the emitter and collector leads 180° apart and the base lead between; and the clockwise configuration of the semicircle looking down at the top of the transistor is C-B-E.

Another method of locating open or shorted transistors is by means of resistance measurements across the elements. Because of differences in transistors and ohmmeters, no specific information can be given about exact resistances. Generally, the ratio forward and backward emitter-collector resistance is between 10:1 and 100:1, the ratio being lower for the higher-powered transistors. When a defective transistor is located, always look for another faulty element in the circuit which may have contributed to or resulted from the transistor failure.

Resistors and capacitors should be checked with one lead unsoldered to avoid any possibility of shunt paths and/or damage to transistors and diodes.

CAUTION

1. USE OF OHMMETER. If an ohmmeter is used to check the forward and reverse resistance of transistors, or to make in-circuit resistance measurements in transistor circuits, check the ohmmeter voltage and current output on the range to be used before making any measurements. Many ohmmeters are unsuitable for use on certain ranges because they supply enough voltage or current to damage a transistor. Check both the open-circuit voltage and the short-circuit current, using suitable test instruments. Do not use any range where open-circuit voltage exceeds 1.5 V or short-circuit current exceeds 3 ma, because these levels may damage transistors.

2. MEASURING TRANSISTOR VOLTAGES. When checking to determine whether a particular transistor is forward-biased, measure the voltage on each lead independently with respect to ground. Do not attempt to measure V_{be} in one step by attaching the voltmeter directly to both leads, because transistor-damaging auxiliary currents may be established.

3. REMOVAL OF PC BOARDS. Read CAUTION note under Paragraph 5.4.1.

5.4.4 USE OF THEORY OF OPERATION. The circuit theory given in Section 4 will be helpful in locating possible causes of trouble. A good understanding of the circuit theory will enable a technician to analyze a particular indication of trouble in terms of possible faulty circuits or components to be checked out.

5.5 PARTS REPLACEMENT

5.5.1 REPLACEMENT OF PARTS ON PRINTED CIRCUIT BOARDS. Parts on all PC boards are identified by silkscreened reference designators. They are shown on the schematics in Section 7. To remove individual components from PC boards, first make a diagram showing exact orientation and connection of the part to simplify future installation. Use a low-power soldering iron (50 watts maximum) and apply heat sparingly to the lead of the part to be replaced. (A suitable way to remove a component is to cut its leads, and then unsolder the ends of the leads that are left in the board.) When removing the device leads, use a toothpick or a small awl to clear the holes of solder. Avoid excessive heat, and always ground the soldering iron to prevent leakage voltage from damaging the component.

When connecting the replacement component, trim the leads so they will penetrate the board about 1/16 inch with the component positioned about 3/16 inch above the board. Hold the part on the component side, and solder the leads from the other side. If possible, hold the component lead on the component side with a tool which will act as a heat sink, such as a pair of needle-nose pliers. Solder with the absolute minimum of heat necessary to completely melt the solder, to avoid overheating. Use a high-quality rosin core solder only; never use paste flux. After soldering, trim off excess leads and flux.

If a break occurs in the etched copper circuit, repair it by soldering a short length of tinned copper wire across the break. Copper that lifts off the board should be cemented in place with a quick-drying acetate base cement having good electrical insulating properties.

5.5.2 REPLACEMENT OF CHASSIS-MOUNTED PARTS. Most parts mounted directly on the chassis or on terminal boards are identified by silkscreened reference designators. Parts not so identified are called out in Figures 5-1 through 5-4 for easy reference. These parts are all shown on the overall schematic diagrams, in Section 7. For soldering work, a 50-watt iron and high-quality rosin core solder should be used. Avoid over heating, and use a pair of needle-nose pliers as a heat sink on the component end of the lead as an extra precaution.

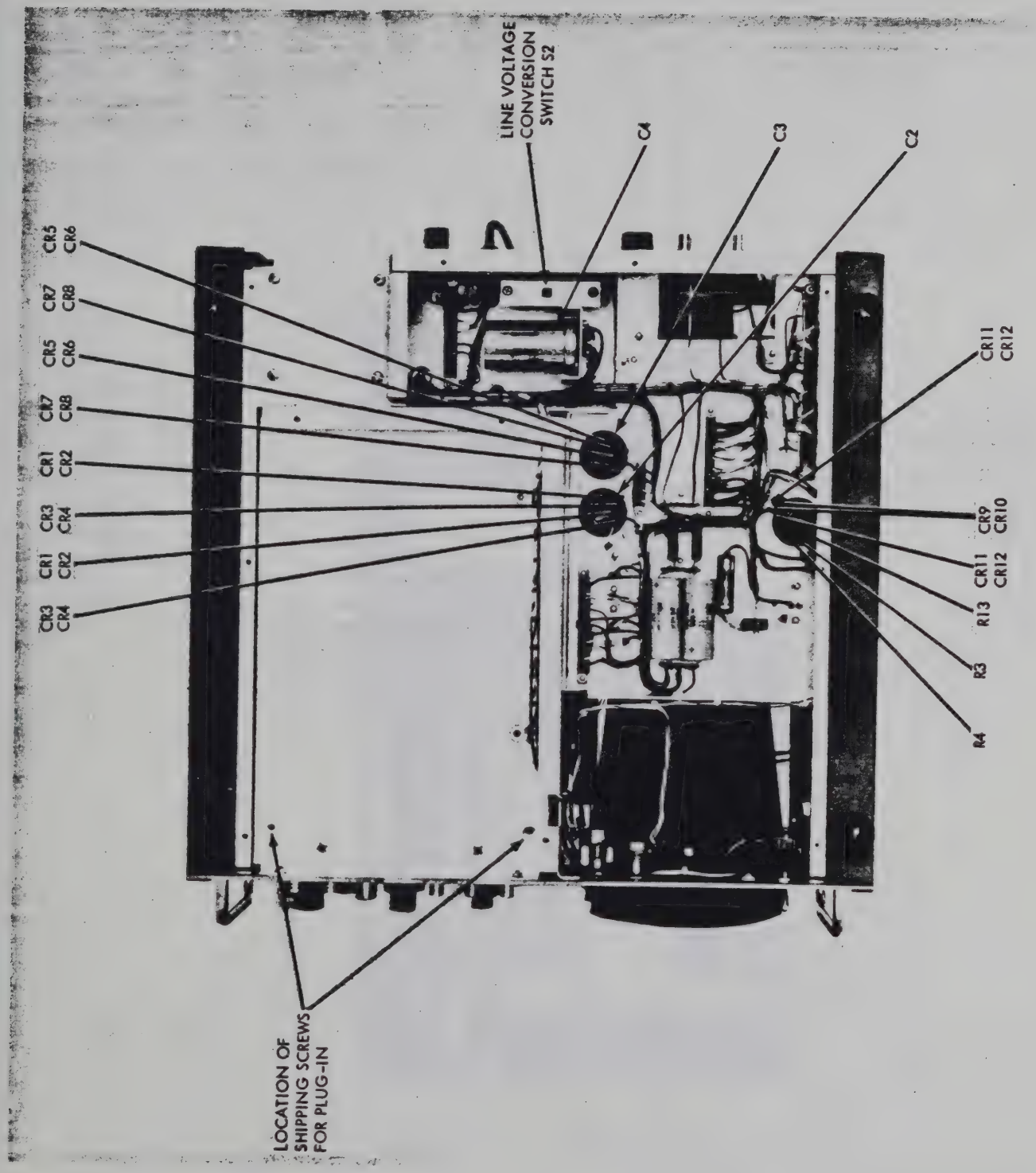


FIGURE 5-2. BOTTOM VIEW OF MODEL 8000 CHASSIS

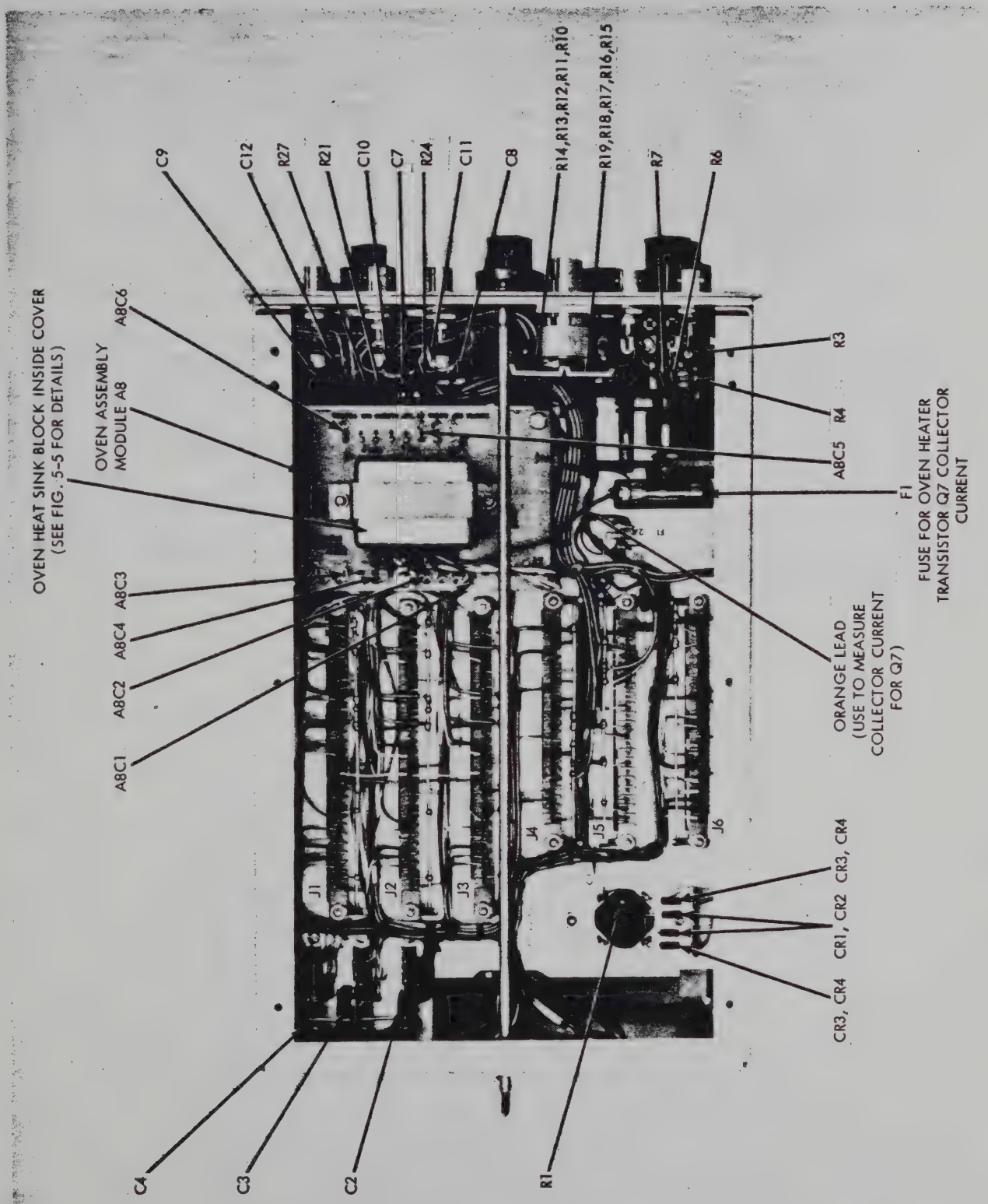


FIGURE 5-3. BOTTOM VIEW OF MODEL 7051 CHASSIS

5.5.3 REPLACEMENT OF PARTS IN OVEN ASSEMBLY MODULE A8. (See Figure 5-5). To replace parts in the oven assembly, disassemble and reassemble as shown in Figure 5-5, in accordance with the following procedure:

NOTE: Access to the leads of transistors mounted in the oven assembly is available on the numbered terminals of the oven assembly PC Board A8 (Fig. 5-3), without requiring disassembly of the oven. Schematic 900823 in Section 7 identifies the transistor connections to each numbered terminal on A8.

a. Remove the oven cover retaining strap, (1, Fig. 5-5), by removing its attaching screws and lockwashers.

b. Lift off the oven cover (2, Fig. 5-5).

c. Remove the one-piece insulator (3, Fig. 5-5).

d. Remove the four mounting screws and standoffs which retain oven assembly PC Board A8 to the Model 7051 chassis, and tilt the board up for access to the oven mounting screws.

e. Remove the two oven block mounting screws and standoffs (4 & 5, Fig. 5-5).

f. Lift off the oven block (6, Fig. 5-5).

g. Unsolder the defective component (lift A8 as necessary for access).

h. If replacing a transistor connected to PC Board A8, clean the PC board holes in accordance with Paragraph 5.8.1 and insert the leads of the new transistor.

i. Place a small amount of silicon grease Heat Conducting Lubricant on the can of the new transistor.

j. Place the oven block over the transistors and install the attaching screws and standoffs (4 & 5, Fig. 5-5).

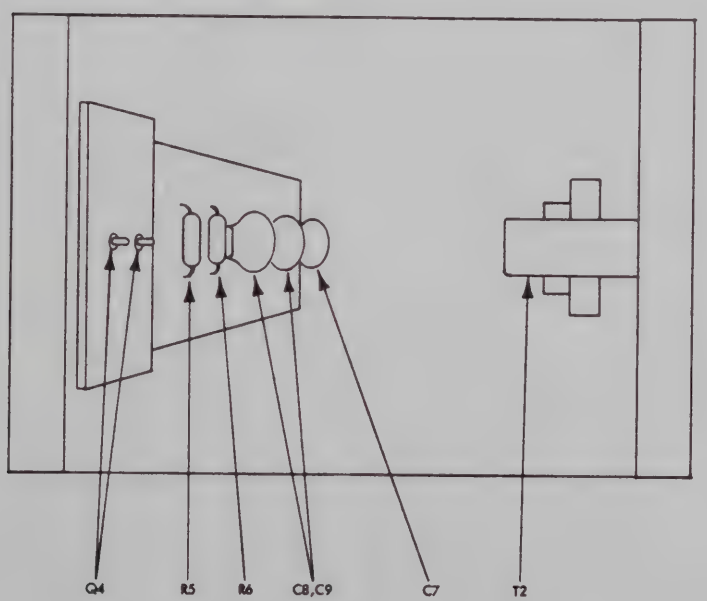
k. Axially press the leads of the new transistor carefully toward the oven block from the printed side of PC board A8, to assure that the can of the new transistor is firmly seated in the oven block.

l. Solder the leads of the new transistor to A8, and then cut off the excess lead length.

m. Tilt the A8 PC board back into place on the Model 7051 chassis and install the four attaching screws and stand offs.

n. Replace the oven cover by the reverse of steps a thru c above.

5.5.4 ADJUSTMENTS REQUIRED AFTER PARTS REPLACEMENT. Refer to Paragraph 5.3 for adjustments after replacement of parts.



NOTE: SEE FIGURE 5-1 FOR GENERAL LOCATION REFERENCE

FIGURE 5-4. LOCATION OF H V SUPPLY COMPONENTS

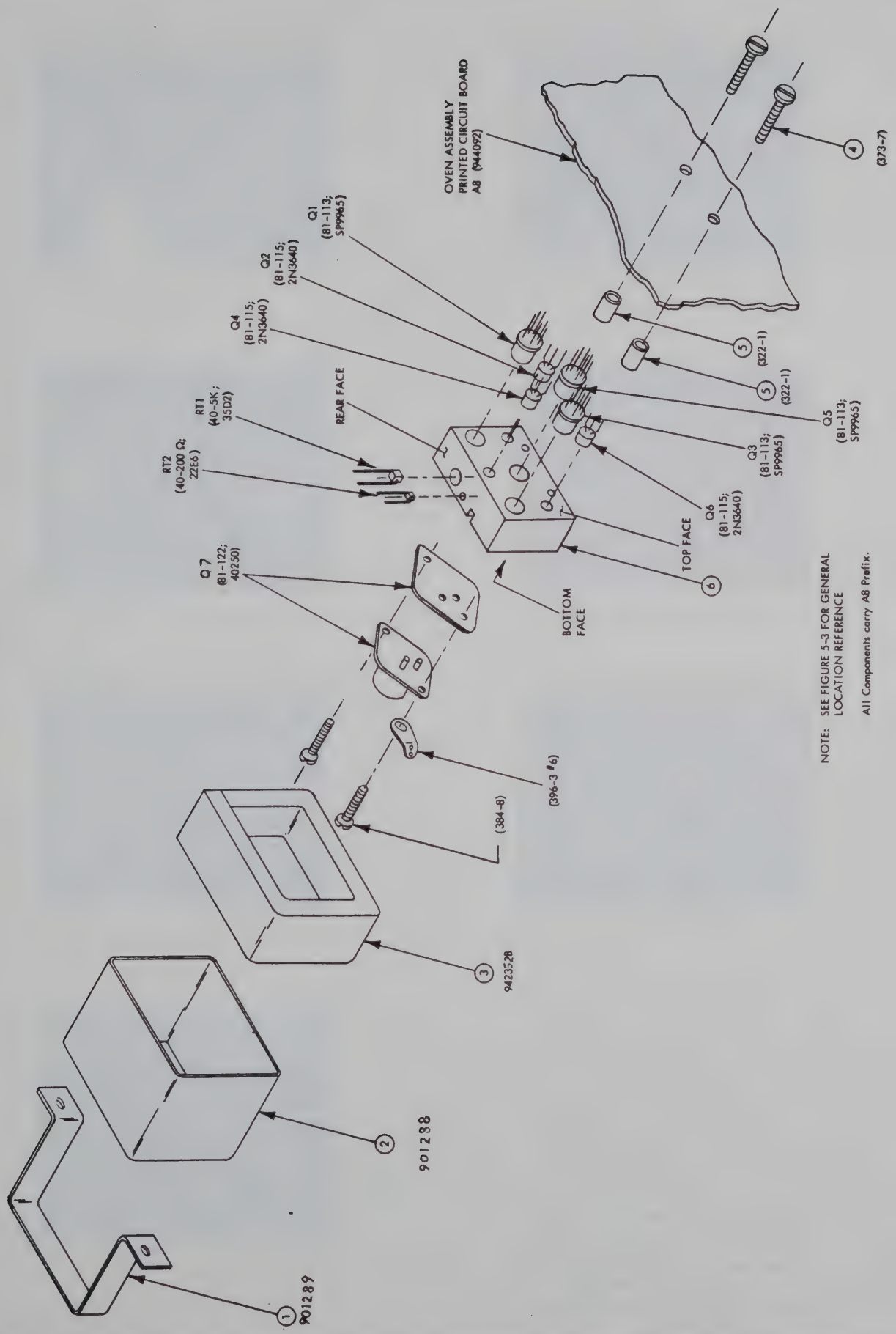
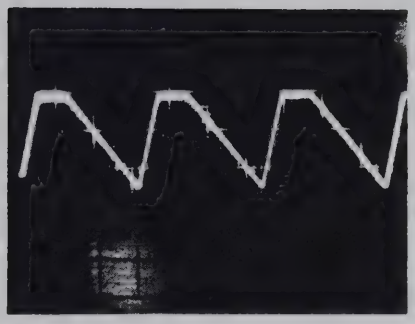
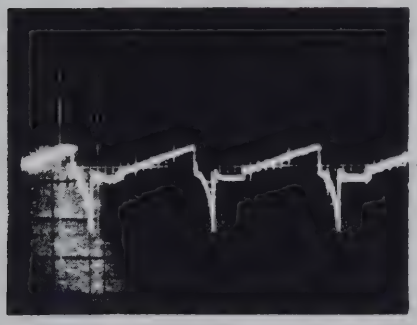


FIGURE 5-5. EXPLODED VIEW OF OVEN HEAT SINK BLOCK SHOWING DISASSEMBLY ORDER AND COMPONENT LOCATIONS

① A6Q1 EMITTER (1 V/cm; DC COUPLING)

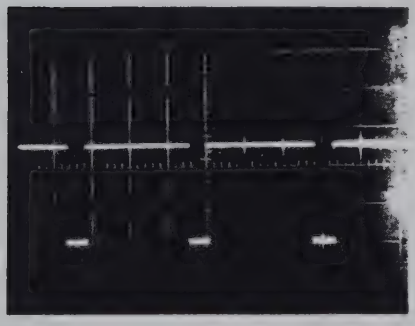


② A6Q2 COLLECTOR (2 V/cm; DC COUPLING)

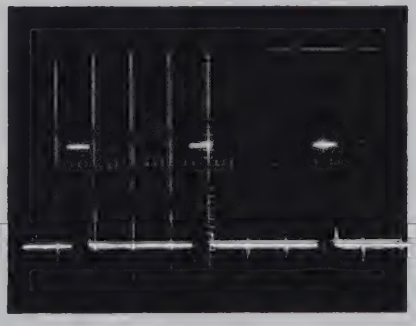


③ A6Q4 BASE (50 mv/cm; AC COUPLING

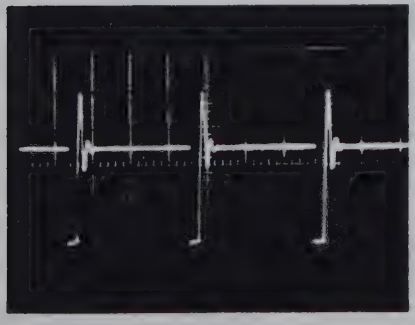
④ A6Q4 COLLECTOR (20 V/cm; DC COUPLING)



⑤ A6Q5 COLLECTOR (5 V/cm; DC COUPLING)



⑥ A6Q6 COLLECTOR (5 V/cm; DC COUPLING)



⑦ A6Q7 COLLECTOR (5 V/cm; DC COUPLING)

NOTE: WAVEFORMS SHOWN WERE OBTAINED UNDER THE FOLLOWING OPERATING CONDITIONS:

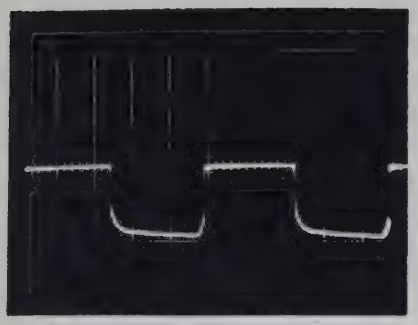
MODEL 8000/7051 CONTROL SETTINGS:
- DISPLAY Mode Selector to LOG A CHN & B CHN
- DISPLAY BALANCE Switch to AUTO
- HORIZONTAL POSITION SENSITIVITY Control to obtain 10 cm sweep width using external sweep input
- CALIBRATOR Switch to OFF, except in #14

OSCILLOSCOPE OPERATING CONDITIONS:
- VERTICAL SENSITIVITY - as indicated on each waveform
- AC OR DC COUPLING - as indicated on each waveform
- HORIZONTAL SWEEP - 5 ms/cm on waveforms 1 - 7 and 13 - 14; 2 µs/cm on waveforms 8 - 12; synced to external sweep source used to drive Model 8000/7051 (OUTPUT BLANKING pulse ALFRED Model 650 Sweep Oscillator)

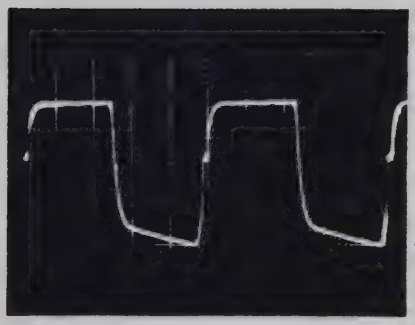
EXTERNAL SWEEP SOURCE APPLIED TO MODEL 8000/7051 INPUT HORIZONTAL JACK:
- OUTPUT SWEEP Signal of ALFRED Model 650 Sweep Oscillator, sweep time 0.01 SEC, synced to LINE

CONNECTIONS TO MODEL 8000/7051 CHN INPUTS JACKS:
- None in #1 - 12; Crystal Detector in #13 & 14

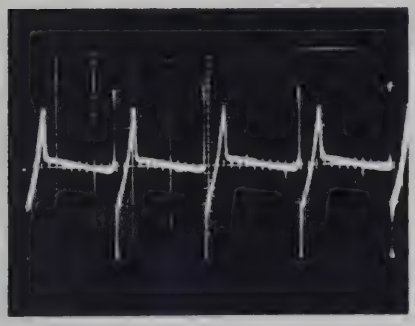
FIGURE 5-6. TYPICAL WAVEFORMS



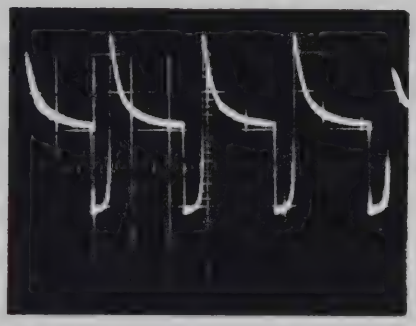
⑧ A5Q9 COLLECTOR (5 V/cm; DC COUPLING)
(A5Q10 COLLECTOR HAS SAME WAVEFORM, INVERTED)



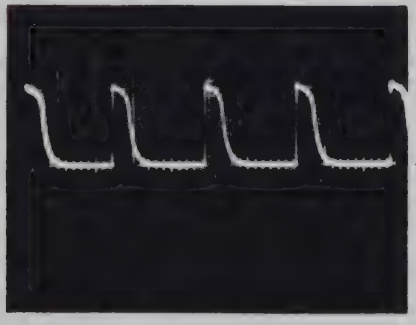
⑨ A5Q3 BASE (0.5 V/cm; AC COUPLING)



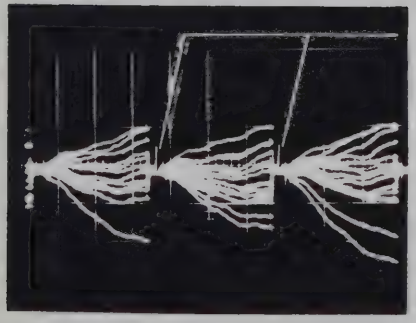
⑩ A5Q11 BASE (1 V/cm; AC COUPLING)



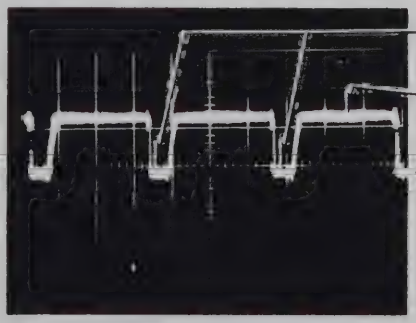
⑪ A5Q11 COLLECTOR (10 V/cm; DC COUPLING)



⑫ TERMINAL A5-T (10 V/cm; DC COUPLING)



⑬ LOG AMPL (A1, A2, A3) TP1 OUTPUT WITH NO SIGNAL INPUT TO CRYSTAL DETECTOR, IN AUTO BALANCE MODE (0.2 V/cm; DC COUPLING; 5 ms/cm HORIZONTAL)



⑭ SAME AS 13 EXCEPT WITH -40 DBM INPUT TO CRYSTAL DETECTOR DETECTOR

FIGURE 5-6. TYPICAL WAVEFORMS (CONT.)

SECTION 6
PARTS LIST

PC BOARD ASSEMBLIES

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION	TOTAL QTY.	PART OF
A1	950998	Channel Amplifier PC Board (For Channel A Signal)	3	Model 7051
A2		Same as A1 (for Channel B Signal)		
A3		Same as A1 (for Channel REF Signal)		
A4	950999	Summing Amplifier PC Board	1	Model 7051
A5	901226	Chopper PC Board	1	Model 7051
A6	901227	Sweep PC Board	1	Model 7051
A7	901228	Calibrator PC Board	1	Model 7051
A8	950950	Oven Assembly (including PC Board A8)	1	Model 7051
A11	950917	High Voltage Regulator & Blanking PC Board	1	Model 8000
A12	950918	High Voltage Rectifier PC Board	1	Model 8000
A13	950915	Low Voltage Supply PC Board	1	Model 8000
A14	950916	CRT Deflection PC Board	1	Model 8000
A15	950997	Calibrator Assembly (including PC Board A7)	1	Model 7051

MODEL 8000 CHASSIS PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
C1	13-23	Capacitor, fixed, elect., 100/100 µf, 200 v
C2 and C3	13-58	Capacitor, fixed, elect., 1000 µf, 50 v
C4	13-56	Capacitor, fixed, elect., 1000/1000 µf, 35 v
C5 and C6	13-60	Capacitor, fixed, elect., 500 µf, 25 v
C7	12-9	Capacitor, fixed, ceramic, .05 µf, 75 v
C8 thru C11	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
CR1 thru CR12	81-20	Diode, D146/1N4385
Q1	81-121	Transistor, 2N3441
Q2 thru Q4	81-122	Transistor, RCA 40250
R1	71-108	Resistor, variable, 25 Ω
R2	43-68 Ω	Resistor, fixed, comp., 68 Ω, 2 w, 10%
R3 and R4	51-100 K	Resistor, fixed, C.F., 100 K, 1/2 w, 5%
R5	51-2.7 K	Resistor, fixed, C.F., 2.7 K, 1/2 w, ± 5%
R6	51-1 K	Resistor, fixed, C.F., 1 K, 1/2 w, ± 5%
R7	71-114	Resistor, variable, 5 K
R8	51-390 Ω	Resistor, fixed, C.F., 390 Ω, 1/2 w, 5%
R9	71-113	Resistor, variable, 100 K
R10 thru R13	51-100 K	Resistor, fixed, C.F., 100 K, 1/2 w, ± 5%
R14	44-1.0 Ω	Resistor, fixed, W.W., 1.0 Ω, 1/2 w, 5%
T1	91-200	Transformer, Power
T2	950964	Transformer, Assembly
S1	101-3	Switch, Toggle DPST
S2	102-136	Switch, Slide DPDT
V1	111-5AQP31A	Tube, Cathode Ray, 5AQP31-A
F1	121-14	Fuse, 2A
F2	121-0.5 A	Fuse, 0.5A
DS1	126-9	Indicator, Panel, red
DS2 thru DS5	126-10	Lamp, #2181
DS6 thru DS9	126-1	Trace Finder Lamp, Neon NE-2
L1 and L2	92-27	Choke, 100 microhy

MODEL 7051 PLUG-IN CHASSIS PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION	
C1	13-58	Capacitor, fixed, elect., 1000 µf, 50 v	
C2	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v	
C3 and C4	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v	
C7 thru C9	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v	
C10 thru C12	12-22	Capacitor, fixed, ceramic, 100 pf	
CR1 thru ~~CR4~~ CR5	81-20	Diode DI46 (or 1N4385)	
R1	51-5.6	Resistor, fixed, C.F., 5.6 K, 1/2 w, 5%	
R2	71-112	Resistor, variable, Dual 10 K - 100 K; with S2	
R3	51-82 K	Resistor, fixed, C.F., 82 K, 1/2 w, 5%	
R4	51-10 K	Resistor, fixed, C.F., 10 K, 1/2 w, 5%	
R5		Same as R2	
R6 and R7	51-100 K	Resistor, fixed, C.F., 100 K, 1/2 w, 5%	
R8 and R9	74-11	Potentiometer, 10 K, 10 turns	
R10	56-10 K	Resistor, fixed, M.F., 10 K, 1/2 w, 1%	
R11	56-20 K	Resistor, fixed, M.F., 20 K, 1/2 w, 1%	
R12	56-49.9 K	Resistor, fixed, M.F., 49.9 K, 1/2 w, 1%	
R13	56-100 K	Resistor, fixed, M.F., 100 K, 1/2 w, 1%	
R14	56-200 K	Resistor, fixed, M.F., 200 K, 1/2 w, 1%	
R15		Same as R10	
R16		Same as R11	
R17		Same as R12	
R18		Same as R13	
R19		Same as R14	
R20	71-116	Resistor, variable, 100 Ω	
R21	51-1 K	Resistor, fixed, C.F., 1 K, 1/2 w, ± 5%	
R22	71-117	Resistor, variable, 20 K	
R23		Same as R20	
R24		Same as R21	
R25		Same as R22	
R26		Same as R20	
R27		Same as R21	
R28		Same as R22	
S1 and S3	102-142	Switch, rotary (7051-101)	
S2	146	See R2	
S4 and S5	102-~~147~~	Switch, rotary, 1PST	
F1	121-1A	Fuse, 2A	
DS1	126-13	Indicator, panel, white, NE-2	

A1/A2/A3 CHANNEL AMPLIFIER PC BOARD ASSEMBLY PARTS *

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A1C1	14-31	Capacitor, fixed, Mylar, .047 µf, 100 v
A1C2	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A1C3	14-30	Capacitor, fixed, Mylar, .1 µf, 100 v
A1C4		Same as A1C2
A1C5		Same as A1C1
A1C6	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A1C7	12-21	Capacitor, fixed, ceramic, 27 pf
A1C8	12-2.2	Capacitor, fixed, ceramic, 2.2 pf, 10%
A1C9		Same as A1C3
A1C10	11-6	Capacitor, fixed, mica, 15 pf, 5%
A1C11 thru A1C13		Same as A1C2
A1C14		Same as A1C6
A1C15		Same as A1C2
A1C16		Same as A1C7
A1C17		Same as A1C6
A1C18		Same as A1C2
A1C19	12-15	Capacitor, fixed, ceramic, .002 µf, 600 v
A1CR1 thru A1CR7	81-41	Diode, 1N459
A1Q1 and A1Q2	81-115	Transistor, 2N3565
A1Q3 and A1Q4	81-114	Transistor, 2N3638A
A1Q5 and A1Q6	81-72	Transistor, 2N699
A1Q7		Same as A1Q1
A1Q8	81-130	Transistor, (FET) U1477/F1313
A1Q9	81-113	Transistor, SP9965
A1Q10		Same as A1Q3
A1Q11	81-127	Transistor, 40321
A1Q12		Same as A1Q3
A1R1	51-100 Ω	Resistor, fixed, carbon film, 100Ω, 1/2 w, ± 5%
A1R2	56-909 K	Resistor, fixed, M.F., 909 K, 1/2 w, ± 1%
A1R3	51-2.7 K	Resistor, fixed, carbon film, 2.7 K, 1/2 w, ± 5%
A1R4		Same as A1R2
A1R5	51-10 K	Resistor, fixed, carbon film, 10 K, 1/2 w, ± 5%
A1R6	56-61.9 K	Resistor, fixed, M.F., 61.9 K, 1/2 w, ± 1%
A1R7	51-270 Ω	Resistor, fixed, carbon film, 270 Ω, 1/2 w, ± 5%
A1R8		Same as A1R6
A1R9		Same as A1R1
A1R10	56-2.87 K	Resistor, fixed, M.F., 2.87 K, 1/2 w, ± 1%
A1R11	51-560 Ω	Resistor, fixed, carbon film, 560 Ω, 1/2 w, ± 5%
A1R12	56-75 K	Resistor, fixed, M.F., 75 K, 1/2 w, ± 1%
A1R13	51-27 Ω	Resistor, fixed, carbon film, 27 Ω, 1/2 w, ± 5%
A1R14		Same as A1R1
A1R15	51-47 K	Resistor, fixed, carbon film, 47 K, 1/2 w, ± 5%
A1R16	51-220 K	Resistor, fixed, carbon film, 220 K, 1/2 w, ± 5%
A1R17	51-120 K	Resistor, fixed, carbon film, 120 K, 1/2 w, ± 5%
A1R18	51-22 K	Resistor, fixed, carbon film, 22 K, 1/2 w, ± 5%
A1R19	51-1 K	Resistor, fixed, carbon film, 1 K, 1/2 w, ± 5%
A1R20 and A1R21	51-4.7 K	Resistor, fixed, carbon film, 4.7 K, 1/2 w, ± 5%
A1R22	71-93	Resistor, variable 10 K, 1 w, 10%
A1R23	41-22 M	Resistor, fixed, comp., 22 M, 1/2 w, ± 10%
A1R24	51-1 M	Resistor, fixed, carbon film, 1 M, 1/2 w, ± 5%
A1R25	56-69.8 K	Resistor, fixed, M.F., 69.8 K, 1/2 w, ± 1%
A1R26*		Resistor, fixed, C.F., 1/2 w, ± 5% Factory selected, nominal value 47 K.
A1R27		Same as A1R1
A1R28	51-1 K	Resistor, fixed, carbon film, 1 K, 1/2 w, ± 5%
A1R29 and A1R30	51-5.6 K	Resistor, fixed, carbon film, 5.6 K, 1/2 w, ± 5%
A1R31 thru A1R33	56-10 K	Resistor, fixed, M.F., 10 K, 1/2 w, ± 1%
A1R34		Same as A1R5
A1R35	71-95	Resistor, variable, 2K
A1R36	56-619 K	Resistor, fixed, M.F., 619 K, 1/2 w, ± 1%
A1R37		Same as A1R5
A1R38	51-56 K	Resistor, fixed, carbon film, 56 K, 1/2 w, 5%
A1R39	51-1 K	Resistor, fixed, carbon film, 1 K, 1/2 w, 5%
A1R40		Same as A1R19
A1R41	51-12 K	Resistor, fixed, carbon film, 12 K, 1/2 w, ± 5%
A1R42		Same as A1R13
A1R43	42-18 K	Resistor, fixed, comp., 18 K, 1 w, ± 10%
A1R44		Same as A1R1
A1R45	56-64.9 K	Resistor, fixed, M.F., 64.9 K, 1/2 w, ± 1%
A1R46		Same as A1R5
A1R47	51-56 K	Resistor, fixed, carbon film, 56 K, 1/2 w, ± 5%
A1R48		Same as A1R1
A1R49	56-17.8 K	Resistor, fixed, M.F., 17.9 K, 1/2 w, ± 1%
A1R50	56-499 Ω	Resistor, fixed, M.F., 499 Ω, 1/2 w, ± 1%
A1R51		Same as A1R41
A1R52	56-9.53 K	Resistor, fixed, M.F., 9.53 K, 1/2 w, ± 1%
A1R53	56-348 K	Resistor, fixed, M.F., 348 K, 1/2 w, ± 1%
A1R54	56-100 K	Resistor, fixed, M.F., 100 K, 1/2 w, ± 1%
A1R55	56-56.2 K	Resistor, fixed, M.F., 56.2 K, 1/2 w, ± 1%
A1R56	56-45.3 K	Resistor, fixed, M.F., 45.3 K, 1/2 w, ± 1%
A1R57	56-187 K	Resistor, fixed, M.F., 187 K, 1/2 w, ± 1%
A1R58	56-86.6 K	Resistor, fixed, M.F., 86.6 K, 1/2 w, ± 1%
A1R59	56-66.5 K	Resistor, fixed, M.F., 66.5 K, 1/2 w, ± 1%
A1R60	51-3.3 K	Resistor, fixed, carbon film, 3.3 K, 1/2 w, 5%
A1R61 and A1R62	51-5.6 K	Resistor, fixed, carbon film, 5.6 K, 1/2 w, 5%
A1K1	106-32	Relay, reed, Wheelock Series 262-1A
A1TP1	133-85	Test point, red

*Factory selected

* Only A1 prefix is shown; A2 and A3 PC Boards are identical.

A4 SUMMING AMPLIFIER PC BOARD ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A4C1 thru A4C6	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A4C7	12-2	Capacitor, fixed, ceramic, .001 µf, 500 v
A4CR1	81-41	Diode, 1N459
A4Q1	81-115	Transistor, 2N3565
A4Q2	81-114	Transistor, 2N3638A
A4Q3	81-72	Transistor, 2N699
A4Q4 thru A4Q6		Same as A4Q1
A4Q7		Same as A4Q2
A4Q8 and A4Q9		Same as A4Q1
A4Q10 thru A4Q12		Same as A4Q2
A4R1	51-27 K	Resistor, fixed, carbon film, 27 K, 1/2 w, ± 5%
A4R2	56-68.1	Resistor, fixed, M.F., 68.1 K, 1/2 w, ± 1%
A4R3	71-111	Resistor, variable, 25 K, ± 30% (CTS)
A4R4	56-6.81 K	Resistor, fixed, M.F., 6.81 K, 1/2 w, ± 1%
A4R5	56-26.1 K	Resistor, fixed, M.F., 26.1 K, 1/2 w, ± 1%
A4R6 and A4R7	56-80.6 K	Resistor, fixed, M.F., 80.6 K, 1/2 w, ± 1%
A4R8	51-15 K	Resistor, fixed, carbon film, 15 K, 1/2 w, ± 5%
A4R9	56-11.8 K	Resistor, fixed, M.F., 11.8 K, 1/2 w, ± 1%
A4R10	51-12 K	Resistor, fixed, carbon film, 12 K, 1/2 w, ± 5%
A4R11	51-4.7 K	Resistor, fixed, carbon film, 4.7 K, 1/2w, ± 5%
A4R12		Same as A4R2
A4R13		Same as A4R3
A4R14		Same as A4R4
A4R15	51-100 Ω	Resistor, fixed, carbon film, 100 Ω, 1/2w, ± 5%
A4R16	43-10 K	Resistor, fixed, comp., 10 K, 2 w, ± 10%
A4R17		Same as A4R3
A4R18	51-10 K	Resistor, fixed, carbon film, 10 K, 1/2w, ± 5%
A4R19	51-47 Ω	Resistor, fixed, carbon film, 47 Ω, 1/2w, ± 5%
A4R20	51-8.2 K	Resistor, fixed, carbon film, 8.2 K, 1/2w, ± 5%
A4R21	51-1.5 K	Resistor, fixed, carbon film, 1.5 K, 1/2 w, ± 5%
A4R22	51-15 Ω	Resistor, fixed, carbon film, 15 Ω, 1/2 w, ± 5%
A4R23		Same as A4R1
A4R24		Same as A4R19
A4R25	56-68.1 K	Resistor, fixed, M.F., 68.1 K, 1/2 w, ± 1%
A4R26		Same as A4R3
A4R27		Same as A4R25
A4R28		Same as A4R15
A4R29		Same as A4R20
A4R30		Same as A4R18
A4R31		Same as A4R21
A4R32		Same as A4R22
A4R33 and A4R34		Same as A4R18

A5 CHOPPER PC BOARD ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A5C1 thru A5C6	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A5C7	12-27	Capacitor, fixed, ceramic, 270 pf, 1000 v
A5C8 and A5C9	14-32	Capacitor, fixed, Mylar, .001 µf, 2%
A5C10		Same as A5C7
A5C11	12-15	Capacitor, fixed, ceramic, .002 µf, 600 v
A5CR1 thru A5CR6	81-27	Diode, 1N625
A5Q1 thru A5Q8	81-115	Transistor, 2N3565
A5Q9 and A5Q10	81-114	Transistor, 2N3638A
A5Q11	81-72	Transistor, 2N699
A5R1	51-18 K	Resistor, fixed, carbon film, 18 K, 1/2 w, ± 5%
A5R2	71-~~102~~ 96	Resistor, variable, 100 Ω, 1/8 w, ± 20%
A5R3	51-820 K	Resistor, fixed, carbon film, 820 K, 1/2 w, ± 5%
A5R4	51-3.3 K	Resistor, fixed, carbon film, 3.3 K, 1/2 w, ± 5%
A5R5	51-12 K	Resistor, fixed, carbon film, 12 K, 1/2 w, ± 5%
A5R6 and A5R7	51-10 K	Resistor, fixed, carbon film, 10 K, 1/2 w, ± 5%
A5R8	56-681 Ω	Resistor, fixed, M.F., 681 Ω, 1/2 w, ± 1%
A5R9	71-~~118~~ 91	Resistor, variable, 500 Ω
A5R10	51-1.5 K	Resistor, fixed, carbon film, 1.5 K, 1/2 w, ± 5%
A5R11	71-~~100~~ 105	Resistor, variable, 1 K
A5R12	51-470 Ω	Resistor, fixed, carbon film, 470 Ω, 1/2 w, ± 5%
A5R13		Same as A5R10
A5R14 and A5R15	51-2.7 K	Resistor, fixed, carbon film, 2.7 K, 1/2 w, ± 5%
A5R16		Same as A5R10
A5R17		Same as A5R11 ok
A5R18		Same as A5R12
A5R19		Same as A5R10
A5R20		Same as A5R9 ok
A5R21		Same as A5R5
A5R22 thru A5R25		Same as A5R6
A5R26	51-5.6 K	Resistor, fixed, carbon film, 5.6 K, 1/2 w, ± 5%
A5R27	56-374 Ω	Resistor, fixed, M.F., 374 Ω, 1/2 w, ± 1%
A5R28		Same as A5R8
A5R29 and A5R30	56-17.8 K	Resistor, fixed, M.F., 17.8 K, 1/2 w, ± 1%
A5R31		Same as A5R27
A5R32		Same as A5R26
A5R33		Same as A5R8
A5R34	51-100 Ω	Resistor, fixed, carbon film, 100 Ω, 1/2 w, ± 5%
A5R35	51-68 Ω	Resistor, fixed, carbon film, 68 ohm, 1/2w, ± 5%
A5R36	51-2.2 K	Resistor, fixed, carbon film, 2.2 K, 1/2 w, ± 5%
A5R37		Same as A5R4
A5R38 thru A5R41	51-56 Ω	Resistor, fixed, carbon film, 56 Ω, 1/2 w, ± 5%
A5R42	51-10 Ω	Resistor, fixed, carbon film, 10 Ω, 1/2 w, ± 5%
A5R43		Same as A5R4
A5R44	51-27 K	Resistor, fixed, carbon film, 27 K, 1/2 w, ± 5%
A5T1	91-202	Transformer (901261B)

A6 SWEEP PC BOARD ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A6C1	12-9	Capacitor, fixed, ceramic, .05 µf, 75 v
A6C2	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A6C3 and A6C4	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A6C5	14-29	Capacitor, fixed, Mylar, .25 µf, 100 v
A6C6		Same as A6C1
A6C7 and A6C8	13-59	Capacitor, fixed, elect., 100 µf, 15 v
A6C9	12-2	Capacitor, fixed, ceramic, .001 µf, 600 v
A6CR1 thru A6CR6	81-41	Diode, 1N459
A6Q1 thru A6Q3	81-115	Transistor, 2N3565
A6Q4	81-72	Transistor, 2N699
A6Q5		Same as A6Q1
A6Q6	81-114	Transistor, 2N3638A
A6Q7		Same as A6Q4
A6Q8		Same as A6Q6
A6Q9 and A6Q10		Same as A6Q1
A6Q11		Same as A6Q6
A6Q12		Same as A6Q1
A6Q13		Same as A6Q4
A6Q14		Same as A6Q1
A6R1	51-33 K	Resistor, fixed, carbon film, 33 K, 1/2 w, ± 5%
A6R2	51-2.7 K	Resistor, fixed, carbon film, 2.7 K, 1/2 w, ± 5%
A6R3	51-47 K	Resistor, fixed, carbon film, 47 K, 1/2 w, ± 5%
A6R4	51-2.2 K	Resistor, fixed, carbon film, 2.2 K, 1/2 w, ± 5%
A6R5	51-39 K	Resistor, fixed, carbon film, 39 K, 1/2 w, ± 5%
A6R6 and A6R7		Same as A6R4
A6R8		Same as A6R1
A6R9	51-8.2 K	Resistor, fixed, carbon film, 8.2 K, 1/2 w, ± 5%
A6R10		Same as A6R4
A6R11	42-22 K	Resistor, fixed, comp., 22 K, 1 w, ± 10%
A6R12	51-120 K	Resistor, fixed, carbon film, 210 K, 1/2 w, ± 5%
A6R13	51-27 K	Resistor, fixed, carbon film, 27 K, 1/2 w, ± 5%
A6R14	51-100 K	Resistor, fixed, carbon film, 100 K, 1/2 w, ± 5%
A6R15 and A6R16	51-10 K	Resistor, fixed, carbon film, 10 K, 1/2 w, ± 5%
A6R17	51-4.7 K	Resistor, fixed, carbon film, 4.7 K, 1/2 w, ± 5%
A6R18		Same as A6R15
A6R19*	51-5.6 K	Resistor, fixed, carbon film, factory-selected, normally 5.6 K, 1/2 w, ± 5%
A6R20	51-5.6 K	Resistor, fixed, carbon film, 5.6 K, 1/2 w, ± 5%
A6R21	51-100 Ω	Resistor, fixed, carbon film, 100 Ω, 1/2 w, ± 5%
A6R22	51-68 K	Resistor, fixed, carbon film, 68 K, 1/2 w, ± 5%
A6R23	56-1.33 K	Resistor, fixed, M.F., 1.33 K, 1/2 w, ± 1%
A6R24	51-330 Ω	Resistor, fixed, carbon film, 330 Ω, 1/2 w, ± 5%
A6R25	51-3.3 K	Resistor, fixed, carbon film, 3.3 K, 1/2 w, ± 5%
A6R26 and A6R27	51-120 Ω	Resistor, fixed, carbon film, 120 Ω, 1/2 w, ± 5%
A6R28		Same as A6R23
A6R29		Same as A6R15
A6R30	51-390 Ω	Resistor, fixed, carbon film, 390 Ω, 1/2 w, ± 5%
A6R31	56-1 K	Resistor, fixed, M.F., 1 K, 1/2 w, ± 1%
A6R32		Same as A6R26
A6R33	51-15 K	Resistor, fixed, carbon film, 15 K, 1/2 w, ± 5%
A6R34	41-6.8 M	Resistor, fixed, carbon film, 6.8 M, 1/2 w, ± 5%
A6R35		Same as A6R14
A6R36		Same as A6R15
A6R37	41-10 M	Resistor, fixed, carbon film, 10 M, 1/2 w, ± 5%
A6R38	51-1 M	Resistor, fixed, carbon film, 1 M, 1/2 w, ± 5%

*Factory-selected

A7 CALIBRATOR PC BOARD ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A7C1	12-2	Capacitor, fixed, ceramic, .001 µf, 600 v
A7C2	12-35	Capacitor, fixed, ceramic, 130 pf, 1 kv
A7C3	11-9	Capacitor, fixed, mica 150 pf, 500 v
A7C4		Same as A7C1
A7C5	11-10	Capacitor, fixed, mica 68 pf, 500 v
A7C6*	12-22	Capacitor, fixed, ceramic, 100 pf, 600 v
A7C7		Same as A7C1
A7Q1	81-105	Transistor, 2N708
A7R1	71-91	Resistor, variable, 500 Ω
A7R2	51-4.7 K	Resistor, fixed, C.F., 4.7 K, 1/2 w, 5%
A7R3	51-27 Ω	Resistor, fixed, C.F., 27 Ω, 1/? w, 5%
A7R4	51-820 Ω	Resistor, fixed, C.F., 820 Ω, 1/2 w, 5%
A7R5	51-15 Ω	Resistor, fixed, carbon film, 15 Ω, 1/2 w, ±5%
A7L1 and A7L2	92-31	Choke, 10 microhy (Gowanda)
A7L3		Not used
A7L4	92-30	Choke, .47 microhy (Gowanda)

A8 OVEN ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A8C1 thru A8C6	12-22	Capacitor, fixed, ceramic, 100 pf
A8Q1	81-113	Transistor, Fairchild SP9965
A8Q2	81-118	Transistor, 2N3640
A8Q3		Same as A8Q1
A8Q4		Same as A8Q2
A8Q5		Same as A8Q1
A8Q6		Same as A8Q2
A8Q7	81-22	Transistor, RCA 40250
A8RT1	40-5 K Ω	Thermistor, Veco 35D2, ± 2%
A8RT2	40-200 Ω	Thermistor, Veco 22E6, ± 10%

*Factory-selected

A11 REGULATOR AND BLANKING PC BOARD PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A11C1	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A11C2	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A11C3 and A11C4		Same as A11C1
A11C5	13-44	Capacitor, fixed, elect., 5 µf, 50 v
A11C6 and A11C7		Same as A11C1
A11C8	12-2	Capacitor, fixed, ceramic, .001 µf, 600 v
A11C9	12-22	Capacitor, fixed, ceramic, 100 pf, 600 v
A11C10		Same as A11C8
A11CR1	81-41	Diode, 1N459
A11Q1 and A11Q2	81-115	Transistor, 2N3565
A11Q3 and A11Q4	81-114	Transistor, 2N3638A
A11Q5	81-72	Transistor, 2N699
A11Q6		Same as A11Q3
A11Q7	81-71	Transistor, 2N697
A11R1	56-95.3 K	Resistor, fixed, M.F., 95.3 K, 1/2 w, 1%
A11R2	51-12 K	Resistor, fixed, C.F., 12 K, 1/2 w, 5%
A11R3	51-68 K	Resistor, fixed, C.F., 68 K, 1/2 w, 5%
A11R4	51-100 Ω	Resistor, fixed, C.F., 100 Ω, 1/2 w, 5%
A11R5	51-1 K	Resistor, fixed, C.F., 1 K, 1/2 w, 10%
A11R6	51-22 K	Resistor, fixed, C.F., 22 K, 1/2 w, 5%
A11R7 and A11R8	43-15 K	Resistor, fixed, comp., 15 K, 2 w, 10%
A11R9	51-3.3 K	Resistor, fixed, C.F., 3.3 K, 1/2 w, 5%
A11R10	56-16.2 K	Resistor, fixed, M.F., 16.2 K, 1/2 w, 1%
A11R11	56-6.19 K	Resistor, fixed, M.F., 6.19 K, 1/2 w, 1%
A11R12	42-5.6 K	Resistor, fixed, comp., 5.6 K, 1 w, 10%
A11R13	51-56 K	Resistor, fixed, C.F., 56 K, 1/2 w, 5%
A11R14	51-100 K	Resistor, fixed, C.F., 100 K, 1/2 w, 5%
A11R15	51-47 Ω	Resistor, fixed, C.F., 47 Ω, 1/2 w, 5%
A11R16	51-10 K	Resistor, fixed, C.F., 10 K, 1/2 w, 5%
A11R17		Same as A11R15
A11R18	51-470 Ω	Resistor, fixed, C.F., 470 Ω, 1/2 w, 5%
A11R19	51-33 K	Resistor, fixed, C.F., 33 K, 1/2 w, 5%
A11R20	51-470 Ω	Resistor, fixed, C.F., 470 Ω, 1/2 w, 5%
A11L1 thru A11L3	92-28	Choke, 100 µh

A12 HIGH VOLTAGE RECTIFIER PC BOARD PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A12C1 thru A12C3	12-33	Capacitor, fixed, ceramic, .01 µf, 3 kv
A12C4	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A12C5 and A12C6		Same as A12C1
A12C7	12-46	Capacitor, fixed, ceramic, 200 pf, 6 kv
A12C8	12-24	Capacitor, fixed, ceramic, 390 pf, 600 v
A12CR1	81-69	Diode, DI1154 EH400
A12CR2 thru A12CR4	81-41	Diode, 1N459
A12R1	51-22 K	Resistor, fixed, C.F., 22 K, 1/2 w, 5%
A12R2	71-109	Resistor, variable, 250 K
A12R3	41-3.3 M	Resistor, fixed, comp., 3.3 M, 1/2 w, 10%
A12R4	71-110	Resistor, variable, 5 M
A12R5 thru A12R9		Same as A12R3
A12R10 thru A12R14	52-3.83 M	Resistor, fixed, M.F., 3.83 M, 1 w, 1%
A12R15	51-27 K	Resistor, fixed, C.F., 27 K, 1/2 w, 5%
A12R16	51-56 K	Resistor, fixed, C.F., 56 K, 1/2 w, 5%
A12R17	51-100 K	Resistor, fixed, C. F., 100 K, 1/2 w, 5%
A12R18	51-220 K	Resistor, fixed, C.F., 220 K, 1/2 w, 5%
A12R19	41-22 M	Resistor, fixed, comp., 22 M, 1/2 w, 10%

A15 CALIBRATOR ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A15C1 and A15C2	12-36	Capacitor, fixed, feedthru, 0.001 µf
A15R1*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 143 Ω
A15R2*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 140 Ω
A15R3 and A15R4	60-140 Ω	Resistor, fixed, M.F., 140 Ω, 1/8 w, 1%
A15R5	60-243 Ω	Resistor, fixed, M.F., 243 Ω, 1/8 w, 1%
A15R6	59-71.5 Ω	Resistor, fixed, M.F., 71.5 Ω, 1/4 w, 1%
A15R7*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 66.5 Ω
A15R8*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 95.3 Ω
A15R9 and A15R10	59-95.3 Ω	Resistor, fixed, M.F., 95.3 Ω, 1/4 w, 1%
A15R11*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 84.5 Ω
A15R12	60-59 Ω	Resistor, fixed, M.F., 59 Ω, 1/8 w, 1%
A15R13*		Resistor, fixed, M.F., 1/8 w, 1% Factory-selected, nominal value 95.3 Ω
A15R14		Same as A15R10
A15R15	51-1 K	Resistor, fixed, C.F., 1 K, 1/2 w, 5%
A15S1	102-143	Switch, Rotary (7051-106)
A7	901228	Calibrator PC Board
		*Factory selected.

A13 LOW VOLTAGE SUPPLY PC BOARD ASSEMBLY PARTS

CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A13C1 and A13C2	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A13C3	14-13	Capacitor, fixed, paper, 1.0 µf, 200 v
A13C4 thru A13C7		Same as A13C1
A13C8	13-40	Capacitor, fixed, elect., 100 µf, 10 v
A13C9		Same as A13C1
A13C10	12-34	Capacitor, fixed, ceramic, 0.1 mf, 100 v
A13C11	12-9	Capacitor, fixed, ceramic, 0.05 µf, 100 v
A13CR1 and A13CR2	81-41	Diode, 1N459
A13CR3	81-75	Diode, Zener, 1N823
A13Q1	81-114	Transistor, 2N3638A
A13Q2	81-72	Transistor, 2N699
A13Q3 and A13Q4	81-115	Transistor, 2N3565
A13Q5	81-71	Transistor, 2N697
A13Q6 and A13Q7		Same as A13Q3
A13Q8		Same as A13Q5
A13Q9 and A13Q10		Same as A13Q3
A13R1	42-22 K	Resistor, fixed, comp., 22 K, 1 w, 10%
A13R2	43-4.7 K	Resistor, fixed, comp., 4.7 K, 2 w, 10%
A13R3	43-10 K	Resistor, fixed, comp., 10 K, 2 w, 10%
A13R4	51-10 Ω	Resistor, fixed, C.F., 10 Ω, 1/2 w, 5%
A13R5	51-1.8 K	Resistor, fixed, C.F., 1.8 K, 1/2 w, 5%
A13R6	51-120 K	Resistor, fixed, C.F., 120 K, 1/2 w, 5%
A13R7	51-5.6 K	Resistor, fixed, C.F., 5.6 K, 1/2 w, 5%
A13R8	51-150 Ω	Resistor, fixed, C.F., 150 Ω, 1/2 w, 5%
A13R9 thru A13R11	56-6.81 K	Resistor, fixed, M.F., 6.81 K, 1/2 w, 1%
A13R12	56-2.05 K	Resistor, fixed, M.F., 2.05 K, 1/2 w, 1%
A13R13	51-220 Ω	Resistor, fixed, C.F., 220 Ω 1/2 w, 5%
A13R14	51-12 K	Resistor, fixed, C.F., 12 K, 1/2 w, 5%
A13R15	51-820 Ω	Resistor, fixed, C.F., 820 Ω, 1/2 w, 5%
A13R16 and A13R17	56-1.54 K	Resistor, fixed, M.F., 1.54 K, 1/2 w, 1%
A13R18		Same as A13R7
A13R19		Same as A13R13
A13R20		Same as A13R14
A13R21	51-10 K	Resistor, fixed, C.F., 10 K, 1/2 w, 5%
A13R22	51-330 Ω	Resistor, fixed, C.F., 330 Ω, 1/2 w, 5%
A13R23	51-680 Ω	Resistor, fixed, C.F., 680 Ω, 1/2 w, 5%
A13R24	51-2.7 K	Resistor, fixed, C.F., 2.7 K, 1/2 w, 5%
A13R25	56-750 Ω	Resistor, fixed, M.F., 750 Ω, 1/2 w, 1%
A13R26	71-90	Resistor, variable, 200 Ω
A13R27		Same as A13R25
A13R28	71-90	Resistor, variable, 200 Ω

A14 CRT DEFLECTION PC BOARD ASSEMBLY PARTS

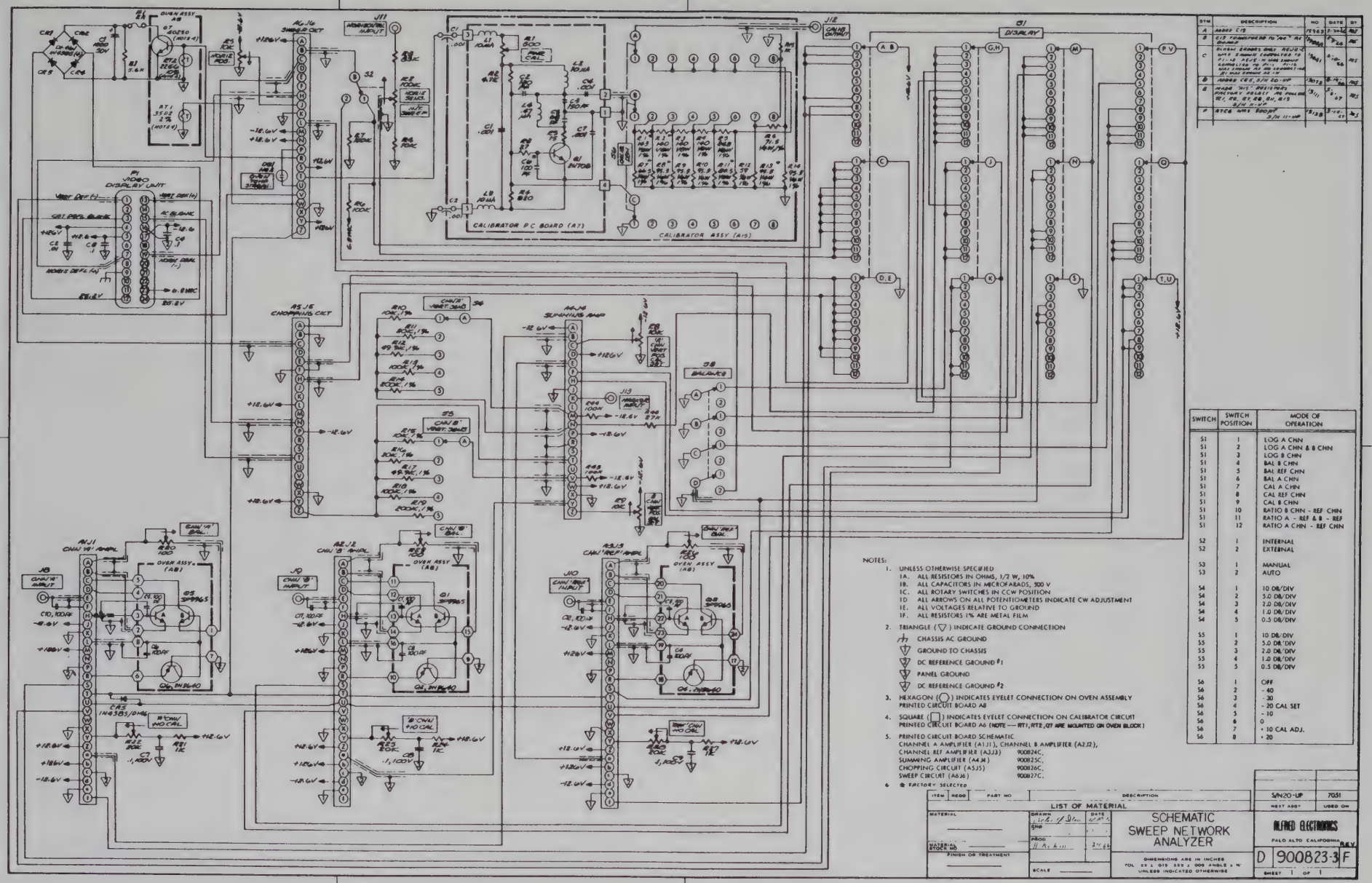
CIRCUIT REFERENCE	ALFRED PART NO.	DESCRIPTION
A14C1	12-3	Capacitor, fixed, ceramic, .01 µf, 600 v
A14C2 thru A14C4	12-34	Capacitor, fixed, ceramic, .1 µf, 100 v
A14C5		Same as A14C1
A14C6 thru A14C8		Same as A14C2
A14CR1 and A14CR2	81-41	Diode, 1N459
A14Q1	81-72	Transistor, 2N699
A14Q2	81-115	Transistor, 2N3565
A14Q3		Same as A14Q1
A14Q4 and A14Q5		Same as A14Q2
A14Q6		Same as A14Q1
A14Q7		Same as A14Q2
A14Q8		Same as A14Q1
A14Q9 and A14Q10		Same as A14Q2
A14Q11 and A14Q12		Same as A14Q1
A14R1	50-10 K	Resistor, fixed, comp., 10 K, 2 w, 2%
A14R2 and A14R3	51-470 Ω	Resistor, fixed, comp., 470 Ω, 1/2 w, 10%
A14R4	51-10 K	Resistor, fixed, C.F., 10 K, 1/2 w, 5%
A14R5	56-4.22 K	Resistor, fixed, M.F., 4.22 K, 1/2 w, 1%
A14R6	56-464 Ω	Resistor, fixed, M.F., 464 Ω, 1/2 w, 1%
A14R7	56-1 K	Resistor, fixed, M.F., 1 K, 1/2 w, 1%
A14R8	71-106	Resistor, variable, 5 K
A14R9		Same as A14R7
A14R10	71-118	Resistor, variable, 500 Ω
A14R11		Same as A14R7
A14R12	56-100 Ω	Resistor, fixed, M.F., 100 Ω, 1/2 w, 1%
A14R13		Same as A14R1
A14R14		Same as A14R4
A14R15		Same as A14R1
A14R16		Same as A14R4
A14R17		Same as A14R5
A14R18		Same as A14R6
A14R19		Same as A14R7
A14R20		Same as A14R8
A14R21		Same as A14R7
A14R22		Same as A14R10
A14R23		Same as A14R7
A14R24		Same as A14R12
A14R25		Same as A14R1
A14R26 thru A14R28		Same as A14R4
A14R29 and A14R30		Same as A14R2
A14R31		Not used
A14R32 and A14R33	51-470 K	Resistor, fixed, C.F., 470 K, 1/2 w, ± 5%
A14R34		Not used
A14R35		Same as A14R32
A14R36 and A14R37	51-270 K	Resistor, fixed, C.F., 270 K, 1/2 w, ± 5%
A14R38 and A14R39		Same as A14R4
A14R40		Same as A14R32
A14R42	51-47 K	Resistor, fixed, C.F., 47 K, 1/2 w, ± 5%
A14R43 and A14R44	51-100 K	Resistor, fixed, C.F., 100 K, 1/2 w, ± 5%
A14R45		Not used
A14R46		Same as A14R42
A14R47 thru A14R50		Same as A14R2
A14L1 thru A14L4	92-29	Choke, rf, 1 millihy

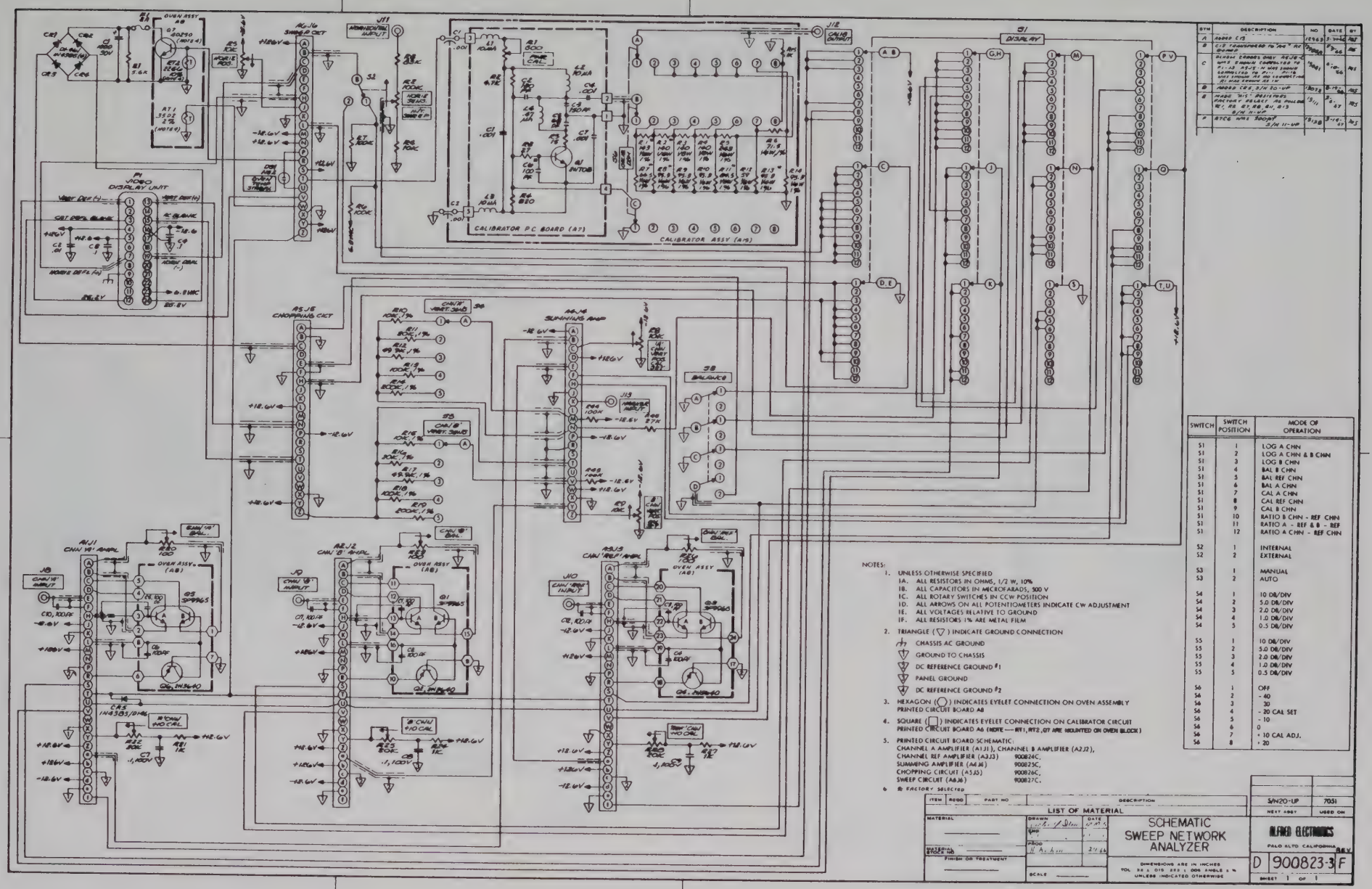
SECTION 7

SCHEMATIC DIAGRAMS

Schematics are included in the following order:

MODEL 7051	SWEEP NETWORK ANALYZER CHASSIS SCHEMATIC	(900823D)
	SIMPLIFIED SCHEMATIC AND WIRING DIAGRAM OF DISPLAY MODE SELECTOR SWITCH S1 AND DISPLAY BALANCE SWITCH S3	(Figure 7-1)
	CHANNEL AMPLIFIER PC BOARD A1/A2/A3	(900824C)
	SUMMING AMPLIFIER PC BOARD A4	(900825C)
	CHOPPING CIRCUIT PC BOARD A5	(900826C)
	SWEEP CIRCUIT PC BOARD A6	(900827C)
MODEL 8000	OSCILLOSCOPE CHASSIS SCHEMATIC	(900804D)
	HIGH VOLTAGE REGULATOR AND BLANKING PC BOARD A11	(900807C)
	LOW VOLTAGE SUPPLIES PC BOARD A13	(900805C)
	DEFLECTION CIRCUIT PC BOARD A14	(900806C)


A1 VIDEO DISPLAY UNIT
A5,J5 CHOPPING CKT
A6,J6 SUMMING AMP
A1,J1 CHAN 'A' AMPL
A2,J2 CHAN 'B' AMPL
A3,J3 CHAN 'REF' AMPL
CALIBRATOR P.C. BOARD (A7)
CALIBRATOR ASSY (A15)
OVEN ASSY A8
A9,J9 SWEEP OUT
J11 HORIZONTAL INPUT
J12 CALIB OUTPUT
J13 VERTICAL INPUT
J8 CHAN 'A' INPUT
J9 CHAN 'B' INPUT
J10 CHAN 'REF' INPUT
S1 VERT. MODE
S2 HORIZ. SOURCE
S3 TRIGGER SOURCE
S4 CHAN 'A' VERT. ZERO
S5 CHAN 'B' VERT. ZERO
S6 BALANCE
A CHAN 'A' GAIN
B CHAN 'B' GAIN
CHAN 'A' BAL.
CHAN 'B' BAL.
CHAN 'REF' BAL.
A CHAN VERT. ZERO
B CHAN VERT. ZERO
A CHAN 'A' NO CAL
B CHAN 'B' NO CAL
CHAN 'REF' NO CAL
HORIZ. ZERO
HORIZ. GAIN
HORIZ. POS.
INTENSITY
FOCUS
ASTIG
TRACE ROTATION
CAL OUTPUT
A CHAN 'A' GAIN
B CHAN 'B' GAIN
A CHAN VERT. ZERO
B CHAN VERT. ZERO
A CHAN 'A' NO CAL
B CHAN 'B' NO CAL
CHAN 'REF' NO CAL
CHAN 'A' BAL.
CHAN 'B' BAL.
CHAN 'REF' BAL.
A CHAN VERT. ZERO
B CHAN VERT. ZERO
A CHAN 'A' NO CAL
B CHAN 'B' NO CAL
CHAN 'REF' NO CAL
A CHAN 'A' GAIN
B CHAN 'B' GAIN



SYM	DESCRIPTION	NO	DATE	BY
A	ADDED C13	1596	3-14-66	RAT
B	C13 TRANSFERRED TO A4 PC BOARD	1596	3-14-66	RAT
C	RESIS. STRIPS ONLY. R6,10 & W13 REMAIN CONNECTED TO P.C. BD. R5,9 W NOW BEING CONNECTED TO P.C. BD. DOES NOT EFFECT A4 PC ASSEMBLY-AB R1 WAS KNOWN AS 1K	1596	3-16-66	RAT
D	ADDED C24, 3/N 20-UP	1578	3-19-66	RAT
E	MARK THIS: RESISTORS FACTORY SELECT AS FOLLOW R1, R4 R7,R8, R11, R13 3/N 11-UP	1578	3-16-66	RAT
F	ATTEN WAS 3900Ω 3/N 11-UP	1578	3-16-66	RAT

SWITCH	SWITCH POSITION	MODE OF OPERATION
S1	1	LOG A CHN
S1	2	LOG A CHN & B CHN
S1	3	LOG B CHN
S1	4	BAL B CHN
S1	5	BAL REF CHN
S1	6	BAL A CHN
S1	7	CAL A CHN
S1	8	CAL REF CHN
S1	9	CAL B CHN
S1	10	RATIO B CHN - REF CHN
S1	11	RATIO A - REF & B - REF
S1	12	RATIO A CHN - REF CHN
S2	1	INTERNAL
S2	2	EXTERNAL
S3	1	MANUAL
S3	2	AUTO
S4	1	10 DB/DIV
S4	2	5.0 DB/DIV
S4	3	2.0 DB/DIV
S4	4	1.0 DB/DIV
S4	5	0.5 DB/DIV
S5	1	10 DB/DIV
S5	2	5.0 DB/DIV
S5	3	2.0 DB/DIV
S5	4	1.0 DB/DIV
S5	5	0.5 DB/DIV
S6	1	OFF
S6	2	- 40
S6	3	- 30
S6	4	- 20 CAL SET
S6	5	- 10
S6	6	0
S6	7	+ 10 CAL ADJ.
S6	8	+ 20

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - 1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1B. ALL CAPACITORS IN MICROFARADS, 500 V
   - 1C. ALL ROTARY SWITCHES IN CCW POSITION
   - 1D. ALL ARROWS ON ALL POTENTIOMETERS INDICATE CW ADJUSTMENT
   - 1E. ALL VOLTAGES RELATIVE TO GROUND
   - 1F. ALL RESISTORS 1% ARE METAL FILM
2. TRIANGLE (▽) INDICATE GROUND CONNECTION
   - CHASSIS AC GROUND
   - GROUND TO CHASSIS
   - DC REFERENCE GROUND #1
   - PANEL GROUND
   - DC REFERENCE GROUND #2
3. HEXAGON (⬡) INDICATES EYELET CONNECTION ON OVEN ASSEMBLY PRINTED CIRCUIT BOARD A8
4. SQUARE (□) INDICATES EYELET CONNECTION ON CALIBRATOR CIRCUIT PRINTED CIRCUIT BOARD A6 (NOTE — RT1, RT2, QT ARE MOUNTED ON OVEN BLOCK)
5. PRINTED CIRCUIT BOARD SCHEMATIC:
   - CHANNEL A AMPLIFIER (A1J1), CHANNEL B AMPLIFIER (A2J2), CHANNEL REF AMPLIFIER (A3J3) 900824C.
   - SUMMING AMPLIFIER (A4J4) 900825C.
   - CHOPPING CIRCUIT (A5J5) 900826C.
   - SWEEP CIRCUIT (A6J6) 900827C.
6. ✱ FACTORY SELECTED

ITEM	REQD	PART NO	DESCRIPTION

LIST OF MATERIAL

SN20-UP	7051
NEXT ASSY	USED ON

MATERIAL

MATERIAL STOCK NO

FINISH OR TREATMENT

DRAWN

CHK

PROD

SCALE

DIMENSIONS ARE IN INCHES
TOL .XX ± .010 .XXX ± .005 ANGLE ± ½
UNLESS INDICATED OTHERWISE

SCHEMATIC
SWEEP NETWORK
ANALYZER

HEWLETT-PACKARD
PALO ALTO CALIFORNIA

D 900823-3 F

SHEET 1 OF 1

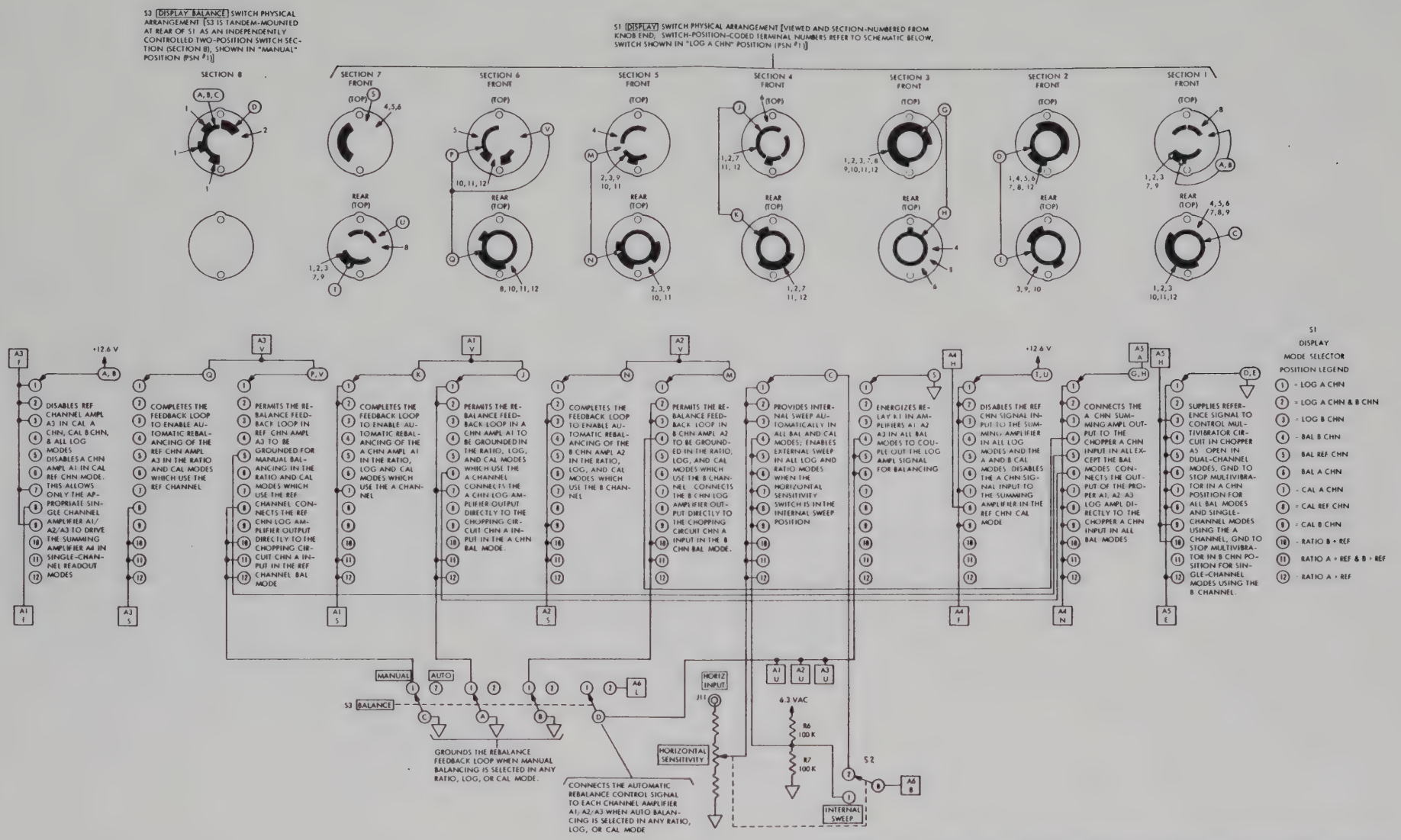

S3 DISPLAY BALANCE SWITCH PHYSICAL ARRANGEMENT [S3 IS TANDEM-MOUNTED AT REAR OF S1 AS AN INDEPENDENTLY CONTROLLED TWO-POSITION SWITCH SECTION (SECTION B), SHOWN IN "MANUAL" POSITION (PSN #1)]
S1 DISPLAY SWITCH PHYSICAL ARRANGEMENT [VIEWED AND SECTION-NUMBERED FROM KNOB END; SWITCH-POSITION-CODED TERMINAL NUMBERS REFER TO SCHEMATIC BELOW, SWITCH SHOWN IN "LOG A CHN" POSITION (PSN #1)]
SECTION B
SECTION 7 FRONT
SECTION 6 FRONT
SECTION 5 FRONT
SECTION 4 FRONT
SECTION 3 FRONT
SECTION 2 FRONT
SECTION 1 FRONT
REAR (TOP)
+12.6 V
DISABLES REF CHANNEL AMPL A3 IN CAL A CHN; CAL B CHN, & ALL LOG MODES
DISABLES A CHN AMPL A1 IN CAL REF CHN MODE. THIS ALLOWS ONLY THE APPROPRIATE SINGLE CHANNEL AMPLIFIER A1/A2/A3 TO DRIVE THE SUMMING AMPLIFIER A4 IN SINGLE-CHANNEL READOUT MODES
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE REF CHN AMPL A3 IN THE RATIO AND CAL MODES WHICH USE THE REF CHANNEL
PERMITS THE REBALANCE FEEDBACK LOOP IN REF CHN AMPL A3 TO BE GROUNDED FOR MANUAL BALANCING IN THE RATIO AND CAL MODES WHICH USE THE REF CHANNEL
CONNECTS THE REF CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE REF CHANNEL BAL MODE
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE A CHN AMPL A1 IN THE RATIO, LOG AND CAL MODES WHICH USE THE A CHANNEL
PERMITS THE REBALANCE FEEDBACK LOOP IN A CHN AMPL A1 TO BE GROUNDED IN THE RATIO, LOG, AND CAL MODES WHICH USE THE A CHANNEL
CONNECTS THE A CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE A CHN BAL MODE.
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE B CHN AMPL A2 IN THE RATIO, LOG, AND CAL MODES WHICH USE THE B CHANNEL
PERMITS THE REBALANCE FEEDBACK LOOP IN B CHN AMPL A2 TO BE GROUNDED IN THE RATIO, LOG, AND CAL MODES WHICH USE THE B CHANNEL. CONNECTS THE B CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE B CHN BAL MODE.
PROVIDES INTERNAL SWEEP AUTOMATICALLY IN ALL BAL AND CAL MODES; ENABLES EXTERNAL SWEEP IN ALL LOG AND RATIO MODES WHEN THE HORIZONTAL SENSITIVITY SWITCH IS IN THE INTERNAL SWEEP POSITION
ENERGIZES RELAY K1 IN AMPLIFIERS A1 A2 A3 IN ALL BAL MODES TO COUPLE OUT THE LOG AMPL SIGNAL FOR BALANCING
DISABLES THE REF CHN SIGNAL INPUT TO THE SUMMING AMPLIFIER IN ALL LOG MODES AND THE A AND B CAL MODES. DISABLES THE A CHN SIGNAL INPUT TO THE SUMMING AMPLIFIER IN THE REF CHN CAL MODE
CONNECTS THE A CHN SUMMING AMPL OUTPUT TO THE CHOPPER A CHN INPUT IN ALL EXCEPT THE BAL MODES. CONNECTS THE OUTPUT OF THE PROPER A1, A2, A3 LOG AMPL DIRECTLY TO THE CHOPPER A CHN INPUT IN ALL BAL MODES
SUPPLIES REFERENCE SIGNAL TO CONTROL MULTIVIBRATOR CIRCUIT IN CHOPPER A3. OPEN IN DUAL-CHANNEL MODES, GND TO STOP MULTIVIBRATOR IN A CHN POSITION FOR ALL BAL MODES AND SINGLE-CHANNEL MODES USING THE A CHANNEL, GND TO STOP MULTIVIBRATOR IN B CHN POSITION FOR SINGLE-CHANNEL MODES USING THE B CHANNEL.
S1 DISPLAY MODE SELECTOR POSITION LEGEND
1 = LOG A CHN
2 = LOG A CHN & B CHN
3 = LOG B CHN
4 = BAL B CHN
5 = BAL REF CHN
6 = BAL A CHN
7 = CAL A CHN
8 = CAL REF CHN
9 = CAL B CHN
10 = RATIO B ÷ REF
11 = RATIO A ÷ REF & B ÷ REF
12 = RATIO A ÷ REF
MANUAL
AUTO
S3 BALANCE
GROUNDS THE REBALANCE FEEDBACK LOOP WHEN MANUAL BALANCING IS SELECTED IN ANY RATIO, LOG, OR CAL MODE.
CONNECTS THE AUTOMATIC REBALANCE CONTROL SIGNAL TO EACH CHANNEL AMPLIFIER A1, A2/A3 WHEN AUTO BALANCING IS SELECTED IN ANY RATIO, LOG, OR CAL MODE
HORIZ INPUT
J11
HORIZONTAL SENSITIVITY
6.3 VAC
R6 100 K
R7 100 K
S2
INTERNAL SWEEP

FIGURE 7-1. SIMPLIFIED SCHEMATIC AND WIRING DIAGRAM OF DISPLAY MODE SELECTOR SWITCH S1 AND DISPLAY BALANCE SWITCH S3

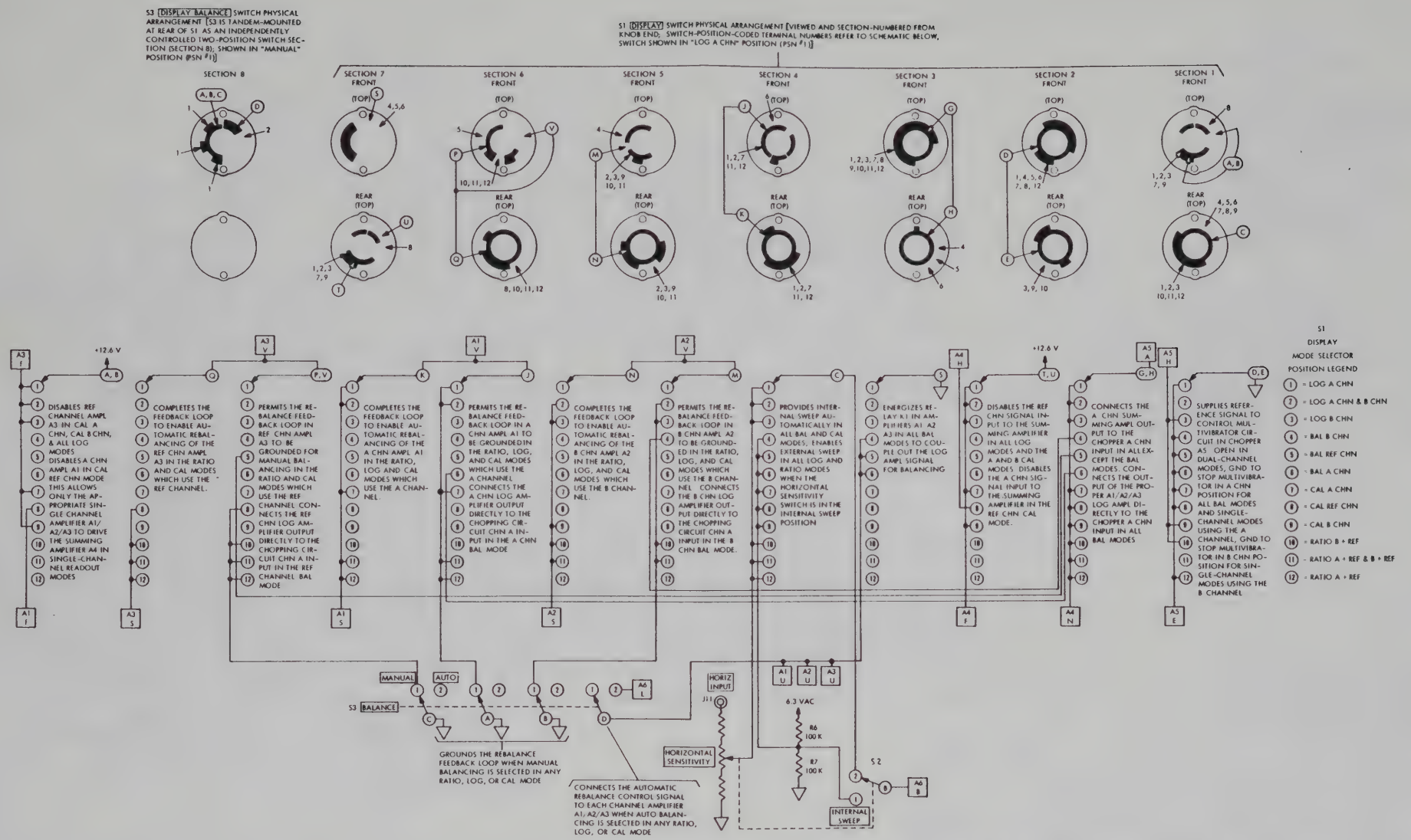
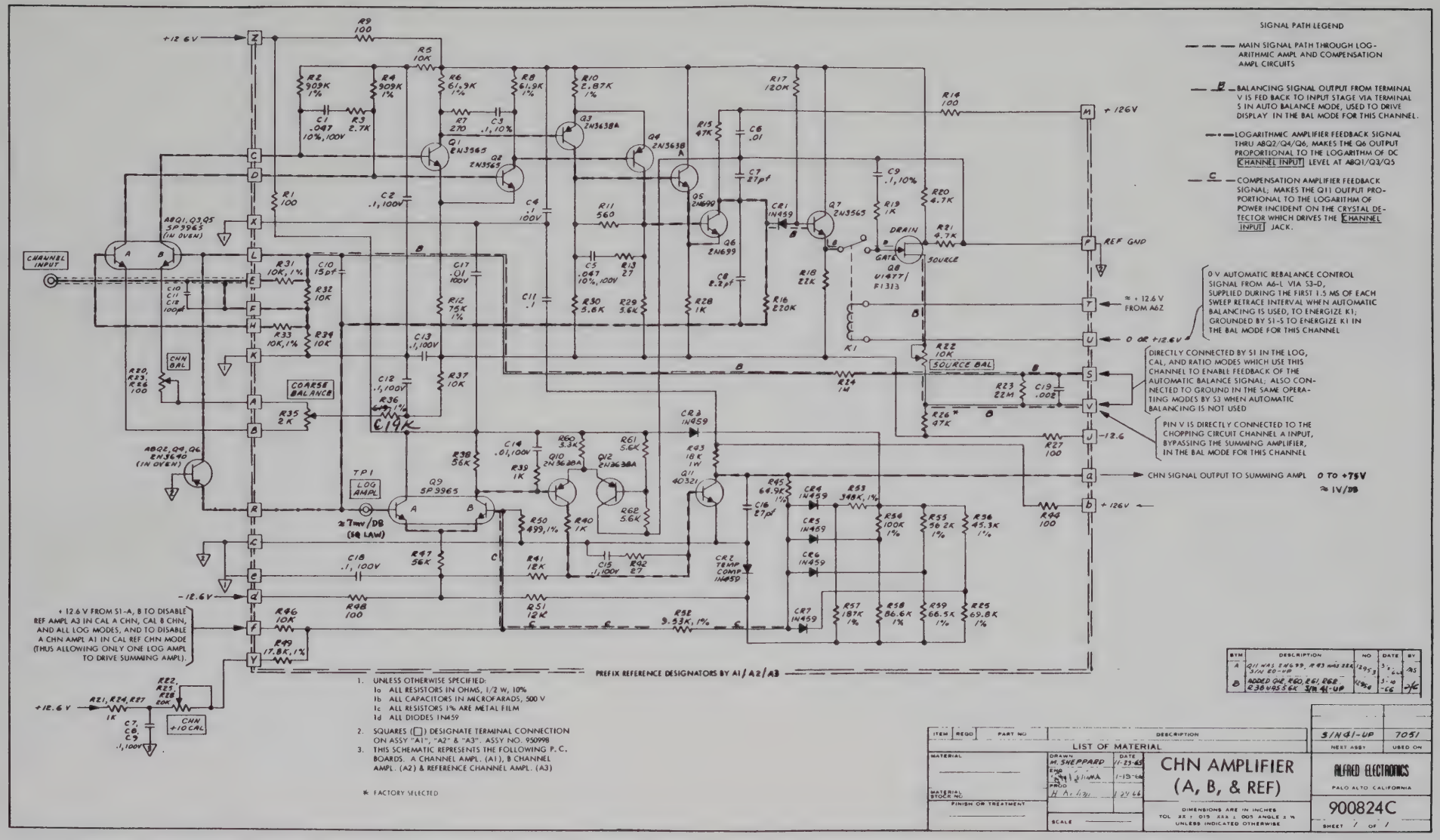

S3 DISPLAY BALANCE SWITCH PHYSICAL ARRANGEMENT [S3 IS TANDEM-MOUNTED AT REAR OF S1 AS AN INDEPENDENTLY CONTROLLED TWO-POSITION SWITCH SECTION (SECTION B); SHOWN IN "MANUAL" POSITION (PSN #1)]
S1 DISPLAY SWITCH PHYSICAL ARRANGEMENT [VIEWED AND SECTION-NUMBERED FROM KNOB END; SWITCH-POSITION-CODED TERMINAL NUMBERS REFER TO SCHEMATIC BELOW, SWITCH SHOWN IN "LOG A CHN" POSITION (PSN #1)]
SECTION B
SECTION 7 FRONT
SECTION 6 FRONT
SECTION 5 FRONT
SECTION 4 FRONT
SECTION 3 FRONT
SECTION 2 FRONT
SECTION 1 FRONT
REAR
DISABLES REF CHANNEL AMPL A3 IN CAL A CHN, CAL B CHN, & ALL LOG MODES DISABLES A CHN AMPL A1 IN CAL REF CHN MODE THIS ALLOWS ONLY THE APPROPRIATE SINGLE CHANNEL AMPLIFIER A1/A2/A3 TO DRIVE THE SUMMING AMPLIFIER A4 IN SINGLE-CHANNEL READOUT MODES
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE REF CHN AMPL A3 IN THE RATIO AND CAL MODES WHICH USE THE REF CHANNEL.
PERMITS THE REBALANCE FEEDBACK LOOP IN REF CHN AMPL A3 TO BE GROUNDED FOR MANUAL BALANCING IN THE RATIO AND CAL MODES WHICH USE THE REF CHANNEL CONNECTS THE REF CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE REF CHANNEL BAL MODE
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE A CHN AMPL A1 IN THE RATIO, LOG AND CAL MODES WHICH USE THE A CHANNEL.
PERMITS THE REBALANCE FEEDBACK LOOP IN A CHN AMPL A1 TO BE GROUNDED IN THE RATIO, LOG, AND CAL MODES WHICH USE THE A CHANNEL CONNECTS THE A CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE A CHN BAL MODE
COMPLETES THE FEEDBACK LOOP TO ENABLE AUTOMATIC REBALANCING OF THE B CHN AMPL A2 IN THE RATIO, LOG, AND CAL MODES WHICH USE THE B CHANNEL.
PERMITS THE REBALANCE FEEDBACK LOOP IN B CHN AMPL A2 TO BE GROUNDED IN THE RATIO, LOG, AND CAL MODES WHICH USE THE B CHANNEL CONNECTS THE B CHN LOG AMPLIFIER OUTPUT DIRECTLY TO THE CHOPPING CIRCUIT CHN A INPUT IN THE B CHN BAL MODE.
PROVIDES INTERNAL SWEEP AUTOMATICALLY IN ALL BAL AND CAL MODES; ENABLES EXTERNAL SWEEP IN ALL LOG AND RATIO MODES WHEN THE HORIZONTAL SENSITIVITY SWITCH IS IN THE INTERNAL SWEEP POSITION
ENERGIZES RELAY K1 IN AMPLIFIERS A1 A2 A3 IN ALL BAL MODES TO COUPLE OUT THE LOG AMPL SIGNAL FOR BALANCING
DISABLES THE REF CHN SIGNAL INPUT TO THE SUMMING AMPLIFIER IN ALL LOG MODES AND THE A AND B CAL MODES DISABLES THE A CHN SIGNAL INPUT TO THE SUMMING AMPLIFIER IN THE REF CHN CAL MODE.
CONNECTS THE A CHN SUMMING AMPL OUTPUT TO THE CHOPPER A CHN INPUT IN ALL EXCEPT THE BAL MODES. CONNECTS THE OUTPUT OF THE PROPER A1/A2/A3 LOG AMPL DIRECTLY TO THE CHOPPER A CHN INPUT IN ALL BAL MODES
SUPPLIES REFERENCE SIGNAL TO CONTROL MULTIVIBRATOR CIRCUIT IN CHOPPER AS OPEN IN DUAL-CHANNEL MODES, GND TO STOP MULTIVIBRATOR IN A CHN POSITION FOR ALL BAL MODES AND SINGLE-CHANNEL MODES USING THE A CHANNEL, GND TO STOP MULTIVIBRATOR IN B CHN POSITION FOR SINGLE-CHANNEL MODES USING THE B CHANNEL
S1 DISPLAY MODE SELECTOR POSITION LEGEND
1 = LOG A CHN
2 = LOG A CHN & B CHN
3 = LOG B CHN
4 = BAL B CHN
5 = BAL REF CHN
6 = BAL A CHN
7 = CAL A CHN
8 = CAL REF CHN
9 = CAL B CHN
10 = RATIO B + REF
11 = RATIO A + REF & B + REF
12 = RATIO A + REF
+12.6 V
MANUAL
AUTO
S3 BALANCE
GROUNDS THE REBALANCE FEEDBACK LOOP WHEN MANUAL BALANCING IS SELECTED IN ANY RATIO, LOG, OR CAL MODE
CONNECTS THE AUTOMATIC REBALANCE CONTROL SIGNAL TO EACH CHANNEL AMPLIFIER A1, A2/A3 WHEN AUTO BALANCING IS SELECTED IN ANY RATIO, LOG, OR CAL MODE
HORIZ INPUT
HORIZONTAL SENSITIVITY
6.3 VAC
R6 100 K
R7 100 K
S2
INTERNAL SWEEP

FIGURE 7-1. SIMPLIFIED SCHEMATIC AND WIRING DIAGRAM OF DISPLAY MODE SELECTOR SWITCH S1 AND DISPLAY BALANCE SWITCH S3


SIGNAL PATH LEGEND
MAIN SIGNAL PATH THROUGH LOGARITHMIC AMPL AND COMPENSATION AMPL CIRCUITS
B — BALANCING SIGNAL OUTPUT FROM TERMINAL V IS FED BACK TO INPUT STAGE VIA TERMINAL S IN AUTO BALANCE MODE, USED TO DRIVE DISPLAY IN THE BAL MODE FOR THIS CHANNEL.
LOGARITHMIC AMPLIFIER FEEDBACK SIGNAL THRU ABQ2/Q4/Q6, MAKES THE Q6 OUTPUT PROPORTIONAL TO THE LOGARITHM OF DC CHANNEL INPUT LEVEL AT ABQ1/Q3/Q5
C — COMPENSATION AMPLIFIER FEEDBACK SIGNAL; MAKES THE Q11 OUTPUT PROPORTIONAL TO THE LOGARITHM OF POWER INCIDENT ON THE CRYSTAL DETECTOR WHICH DRIVES THE CHANNEL INPUT JACK.
+12.6V
+126V
REF GND
≈ +12.6V FROM A6Z
0 OR +12.6V
0 V AUTOMATIC REBALANCE CONTROL SIGNAL FROM A6-L VIA S3-D, SUPPLIED DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL WHEN AUTOMATIC BALANCING IS USED, TO ENERGIZE K1; GROUNDED BY S1-S TO ENERGIZE K1 IN THE BAL MODE FOR THIS CHANNEL
DIRECTLY CONNECTED BY S1 IN THE LOG, CAL, AND RATIO MODES WHICH USE THIS CHANNEL TO ENABLE FEEDBACK OF THE AUTOMATIC BALANCE SIGNAL; ALSO CONNECTED TO GROUND IN THE SAME OPERATING MODES BY S3 WHEN AUTOMATIC BALANCING IS NOT USED
PIN V IS DIRECTLY CONNECTED TO THE CHOPPING CIRCUIT CHANNEL A INPUT, BYPASSING THE SUMMING AMPLIFIER, IN THE BAL MODE FOR THIS CHANNEL
-12.6
CHN SIGNAL OUTPUT TO SUMMING AMPL 0 TO +7.5V ≈ 1V/DB
+126V
CHANNEL INPUT
ABQ1, Q3, Q5 5P3965 (IN OVEN)
ABQ2, Q4, Q6 2N3690 (IN OVEN)
CHN BAL
R20, R23, R28 100
COARSE BALANCE
R35 2K
C19K
TP1
LOG AMPL
≈ 7mv/DB (SQ LAW)
Q9 5P3965
Q1 2N3565
Q2 2N3565
Q3 2N3638A
Q4 2N3638A
Q5 2N699
Q6 2N699
Q7 2N3565
Q8 U1877/ F1313
DRAIN
GATE
SOURCE
K1
SOURCE BAL
Q10 2N3638A
Q12 2N3638A
Q11 40321
CR1 1N459
CR2 1N459
CR2 TEMP COMP 1N459
CR3 1N459
CR4 1N459
CR5 1N459
CR6 1N459
CR7 1N459
+12.6V FROM S1-A, B TO DISABLE REF AMPL A3 IN CAL A CHN, CAL B CHN, AND ALL LOG MODES, AND TO DISABLE A CHN AMPL A1 IN CAL REF CHN MODE (THUS ALLOWING ONLY ONE LOG AMPL TO DRIVE SUMMING AMPL).
A21, R24, R27 1K
R22, R25, R28 10K
CHN +10 CAL
C7, C8, C9 .1, 100V
PREFIX REFERENCE DESIGNATORS BY A1/A2/A3

1. UNLESS OTHERWISE SPECIFIED:
   - 1a ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1b ALL CAPACITORS IN MICROFARADS, 500 V
   - 1c ALL RESISTORS 1% ARE METAL FILM
   - 1d ALL DIODES 1N459
2. SQUARES (□) DESIGNATE TERMINAL CONNECTION ON ASSY "A1", "A2" & "A3". ASSY NO. 950998
3. THIS SCHEMATIC REPRESENTS THE FOLLOWING P. C. BOARDS. A CHANNEL AMPL. (A1), B CHANNEL AMPL. (A2) & REFERENCE CHANNEL AMPL. (A3)

* FACTORY SELECTED

BYN	DESCRIPTION	NO	DATE	BY
A	Q11 WAS 2N699, R93 WAS 22K, S/N 80-UP	2955	3-10-66	RS
B	ADDED CR8, R60, R61, R62, R38 WAS 56K, R93 WAS 18K S/N 91-UP	4284	3-10-66	JHC

ITEM	REQD	PART NO	DESCRIPTION
			LIST OF MATERIAL

MATERIAL

MATERIAL STOCK NO.

FINISH OR TREATMENT

DRAWN	M. SHEPPARD	1-23-66
ENG	[illegible]	1-19-66
PROD	[illegible]	1-24-66

SCALE

DIMENSIONS ARE IN INCHES
TOL .XX ± .015 .XXX ± .005 ANGLE ± 1°
UNLESS INDICATED OTHERWISE

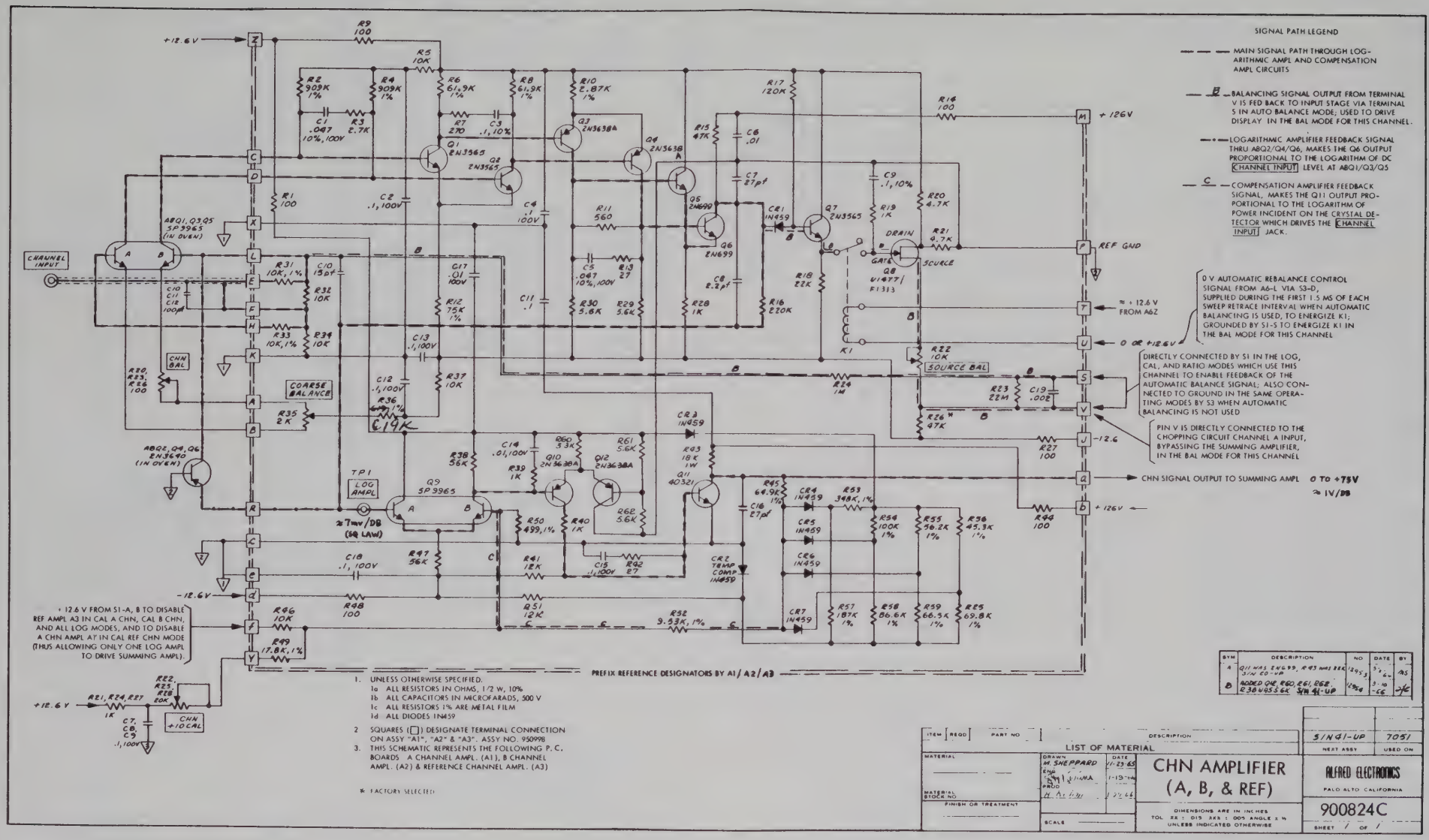
CHN AMPLIFIER (A, B, & REF)

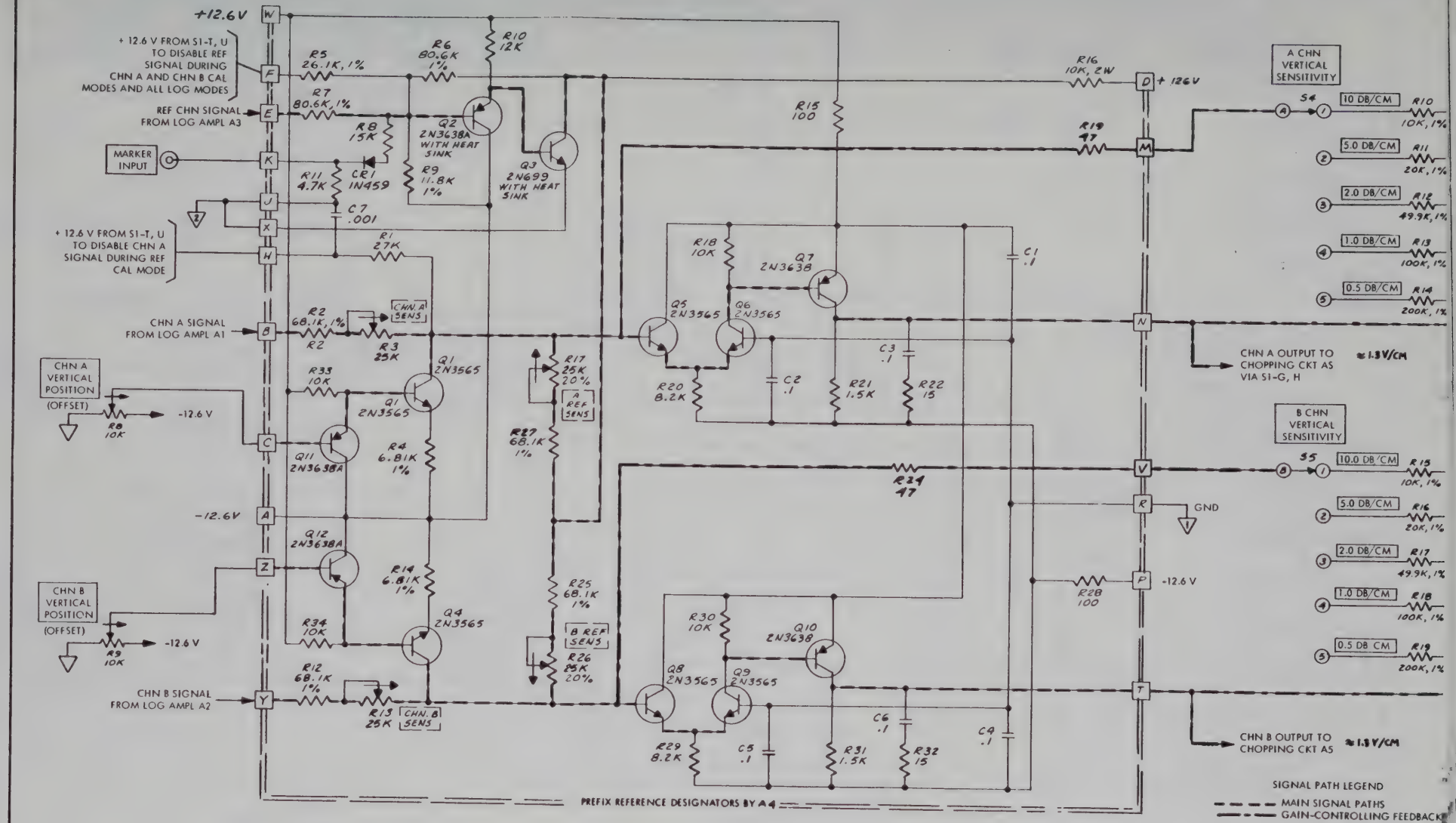
S/N 91-UP	7051
NEXT ASSY	USED ON

ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900824C

SHEET 1 OF 1


SIGNAL PATH LEGEND
MAIN SIGNAL PATH THROUGH LOGARITHMIC AMPL AND COMPENSATION AMPL CIRCUITS
B — BALANCING SIGNAL OUTPUT FROM TERMINAL V IS FED BACK TO INPUT STAGE VIA TERMINAL S IN AUTO BALANCE MODE; USED TO DRIVE DISPLAY IN THE BAL MODE FOR THIS CHANNEL.
LOGARITHMIC AMPLIFIER FEEDBACK SIGNAL THRU ABQ2/Q4/Q6; MAKES THE Q6 OUTPUT PROPORTIONAL TO THE LOGARITHM OF DC CHANNEL INPUT LEVEL AT ABQ1/Q3/Q5
C — COMPENSATION AMPLIFIER FEEDBACK SIGNAL, MAKES THE Q11 OUTPUT PROPORTIONAL TO THE LOGARITHM OF POWER INCIDENT ON THE CRYSTAL DETECTOR WHICH DRIVES THE CHANNEL INPUT JACK.
+12.6 V
CHANNEL INPUT
ABQ1, Q3, Q5 SP3965 (IN OVEN)
ABQ2, Q4, Q6 2N3640 (IN OVEN)
CHN BAL
COARSE BALANCE
LOG AMPL
TP1
≈ 7mv/DB (SQ LAW)
Q1 2N3565
Q2 2N3565
Q3 2N3638A
Q4 2N3638A
Q5 2N699
Q6 2N699
Q7 2N3565
Q8 U1477/F1313
Q9 SP3965
Q10 2N3638A
Q11 40321
Q12 2N3638A
CR1 IN459
CR2 IN459
CR2 TEMP COMP IN459
CR3 IN459
CR4 IN459
CR5 IN459
CR6 IN459
CR7 IN459
K1
DRAIN
GATE
SOURCE
SOURCE BAL
REF GND
≈ +12.6 V FROM A6Z
0 OR +12.6V
0 V AUTOMATIC REBALANCE CONTROL SIGNAL FROM A6-L VIA S3-D, SUPPLIED DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL WHEN AUTOMATIC BALANCING IS USED; TO ENERGIZE K1; GROUNDED BY S1-S TO ENERGIZE K1 IN THE BAL MODE FOR THIS CHANNEL
DIRECTLY CONNECTED BY S1 IN THE LOG, CAL, AND RATIO MODES WHICH USE THIS CHANNEL TO ENABLE FEEDBACK OF THE AUTOMATIC BALANCE SIGNAL; ALSO CONNECTED TO GROUND IN THE SAME OPERATING MODES BY S3 WHEN AUTOMATIC BALANCING IS NOT USED
PIN V IS DIRECTLY CONNECTED TO THE CHOPPING CIRCUIT CHANNEL A INPUT, BYPASSING THE SUMMING AMPLIFIER, IN THE BAL MODE FOR THIS CHANNEL
CHN SIGNAL OUTPUT TO SUMMING AMPL
0 TO +7.5V ≈ 1V/DB
-12.6
-12.6 V
+12.6 V FROM S1-A, B TO DISABLE REF AMPL A3 IN CAL A CHN, CAL B CHN, AND ALL LOG MODES, AND TO DISABLE A CHN AMPL A1 IN CAL REF CHN MODE (THUS ALLOWING ONLY ONE LOG AMPL TO DRIVE SUMMING AMPL).
CHN +/OCAL
C19 .002
C14 .01,100V
C16 27pf
C17 .01 100V
C18 .1, 100V
C13 .1,100V
C12 .1,100V
C10 15pf
C11 .1
C15 .1,100V
C7 27pf
C8 2.2pf
C9 .1, 10%
C5 .047 10%,100V
C6 .01
C4 .1 100V
C2 .1, 100V
C1 .047 10%,100V
R1 100
R2 909K 1%
R3 2.7K
R4 909K 1%
R5 10K
R6 61.9K 1%
R7 270
R8 61.9K 1%
R9 100
R10 2.87K 1%
R11 560
R12 75K 1%
R13 27
R14 100
R15 47K
R16 220K
R17 120K
R18 22K
R19 1K
R20 4.7K
R21 4.7K
R22 10K
R23 22M
R24 1M
R25 69.8K 1%
R26 47K
R27 100
R28 1K
R29 5.6K
R30 5.6K
R31 10K, 1%
R32 10K
R33 10K, 1%
R34 10K
R35 2K
R36 6.19K 1%
R37 10K
R38 56K
R39 1K
R40 1K
R41 12K
R42 E7
R43 18K 1W
R44 100
R45 64.9K 1%
R46 10K
R47 56K
R48 100
R49 17.8K, 1%
R50 499, 1%
R51 12K
R52 9.53K, 1%
R53 348K, 1%
R54 100K 1%
R55 50.2K 1%
R56 45.3K 1%
R57 187K 1%
R58 86.6K 1%
R59 66.5K 1%
R60 3.3K
R61 5.6K
R62 5.6K
R20, R23, R26 100
R21, R24, R27 1K
R22, R25, R28 20K
C7, C8, C9 .1,100V
PREFIX REFERENCE DESIGNATORS BY A1/A2/A3
1. UNLESS OTHERWISE SPECIFIED.
1a ALL RESISTORS IN OHMS, 1/2 W, 10%
1b ALL CAPACITORS IN MICROFARADS, 500 V
1c ALL RESISTORS 1% ARE METAL FILM
1d ALL DIODES IN459
2 SQUARES (□) DESIGNATE TERMINAL CONNECTION ON ASSY "A1", "A2" & "A3". ASSY NO. 950998
3. THIS SCHEMATIC REPRESENTS THE FOLLOWING P.C. BOARDS: A CHANNEL AMPL. (A1), B CHANNEL AMPL. (A2) & REFERENCE CHANNEL AMPL. (A3)
* FACTORY SELECTED
SYM DESCRIPTION NO DATE BY
A Q11 WAS 2N699, R43 WAS 22K; J-W TO +V 1295 5-64 AS
B ADDED Q12, R60, R61, R62, R38 WAS 56K SN 61-UP 1456 3-66 JK
ITEM REQD PART NO DESCRIPTION
LIST OF MATERIAL
S/N 61-UP 7051
NEXT ASSY USED ON
MATERIAL
FINISH OR TREATMENT
DRAWN M. SHEPPARD 11-23-65
ENG
PROD
SCALE
CHN AMPLIFIER (A, B, & REF)
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA
900824C
DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE
SHEET 1 OF 1



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   1B. ALL CAPACITORS IN MICROFARADS, 500 V.
   1C. ALL RESISTORS 1% ARE METAL FILM.
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A4" ASSY NO. 950999.

LIST OF MATERIAL

ITEM	REQD	PART NO	DESCRIPTION

MATERIAL
MATERIAL STOCK NO
FINISH OR TREATMENT
DRAWN M. SHEPPARD DATE 11-17-65
ENG
PROD
SCALE
DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE

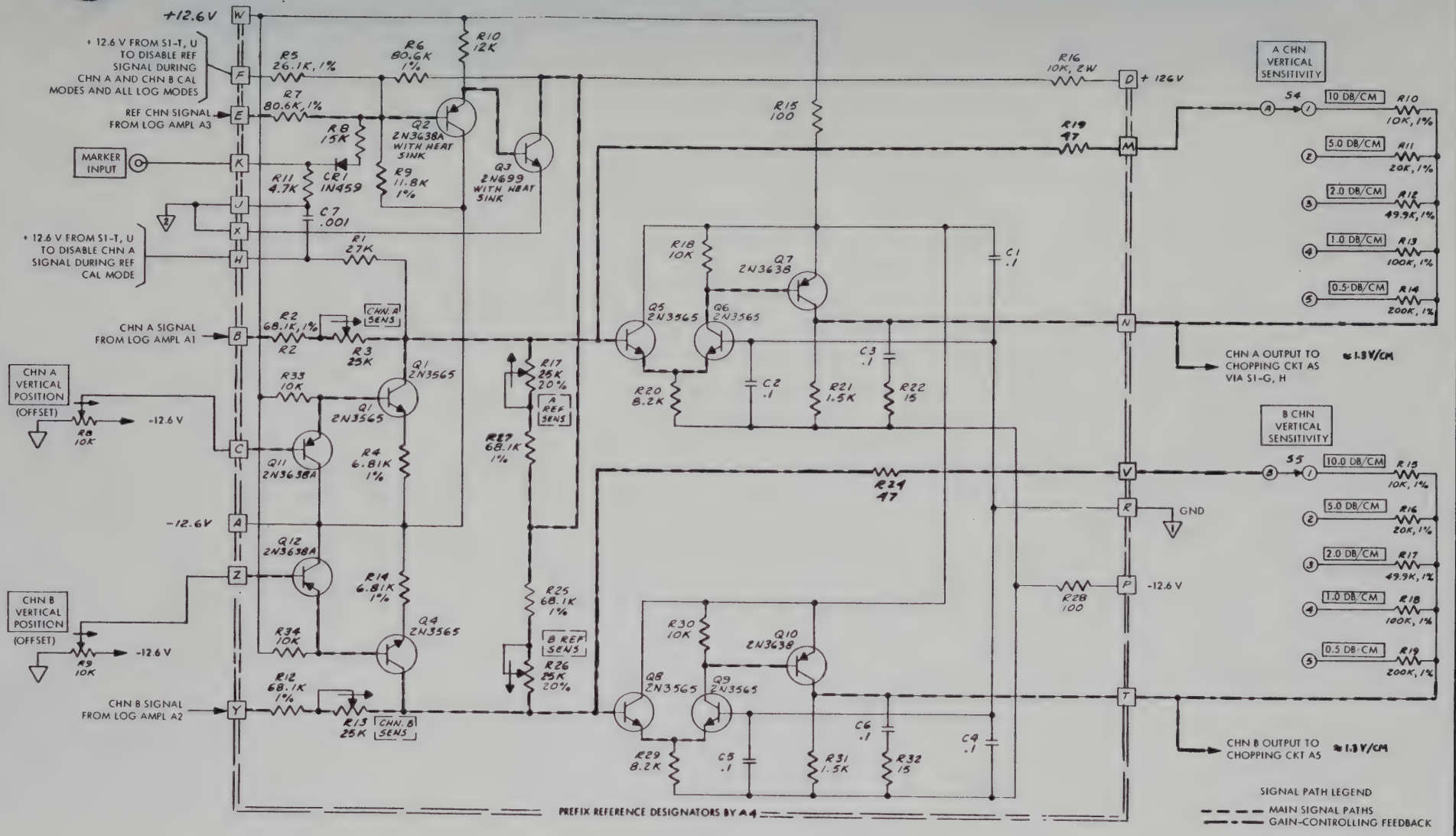
SUMMING AMPLIFIER

S/N 20-up
NEXT ASSY
USED 7051

ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900825C-1

SHEET 1 OF 1



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   1B. ALL CAPACITORS IN MICROFARADS, 500 V.
   1C. ALL RESISTORS 1% ARE METAL FILM.
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A4" ASSY NO. 950999.

ITEM	REQD	PART NO	DESCRIPTION
			LIST OF MATERIAL

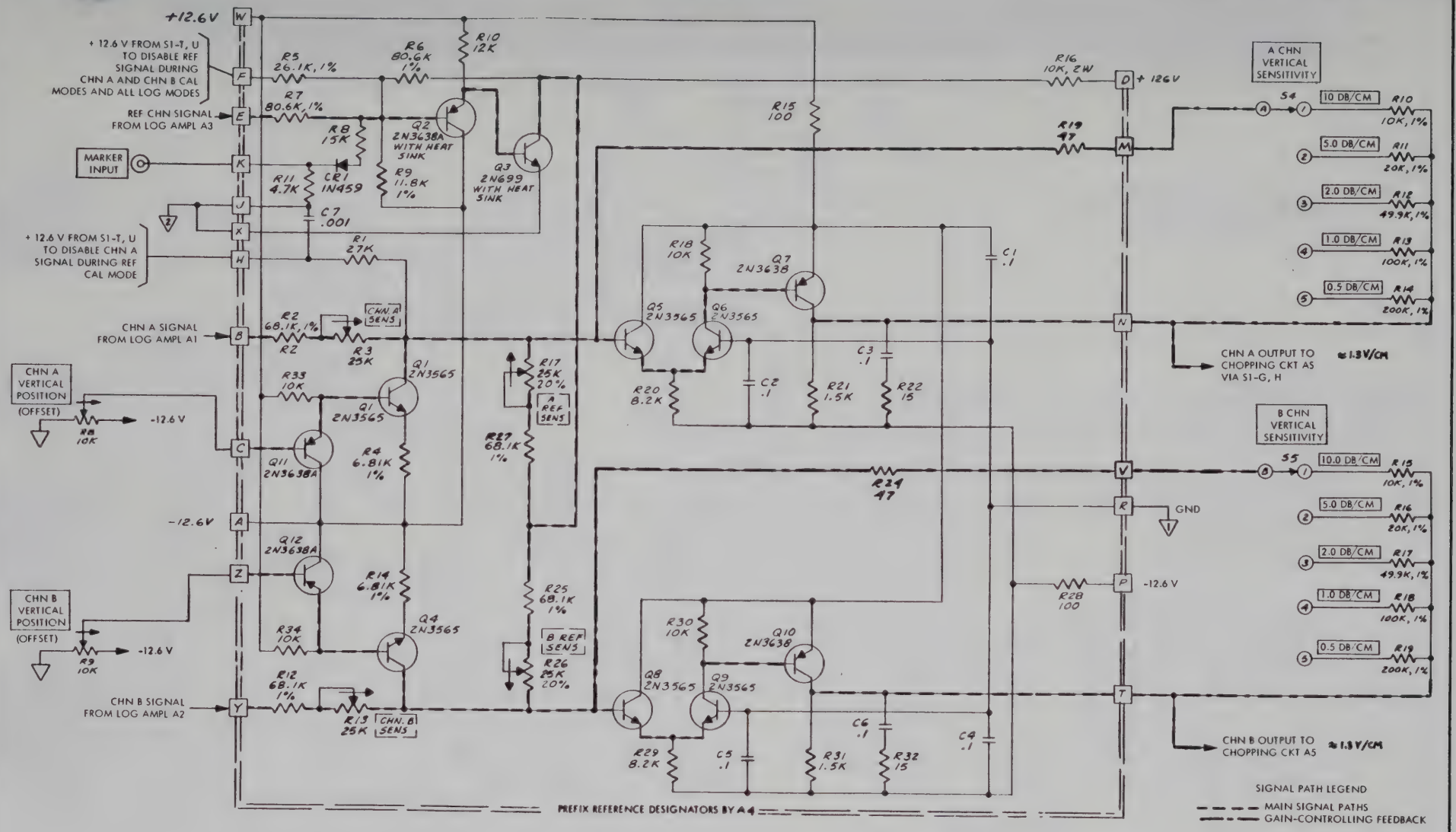
MATERIAL	DRAWN M. SHEPPARD	DATE 11-17-65	SUMMING AMPLIFIER
MATERIAL STOCK NO	ENG		
FINISH OR TREATMENT	PROD		DIMENSIONS ARE IN INCHES TOL XX ± .015 XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE
	SCALE		

S/N 20-110	7051
NEXT ASSY	USED ON

ALFRED ELECTRONICS
PALO ALTO, CALIFORNIA

900825C-1

SHEET 1 OF 1



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - 1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1B. ALL CAPACITORS IN MICROFARADS, 500 V.
   - 1C. ALL RESISTORS 1% ARE METAL FILM.
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A4" ASSY NO. 950999.

ITEM	REQD	PART NO	DESCRIPTION
			LIST OF MATERIAL

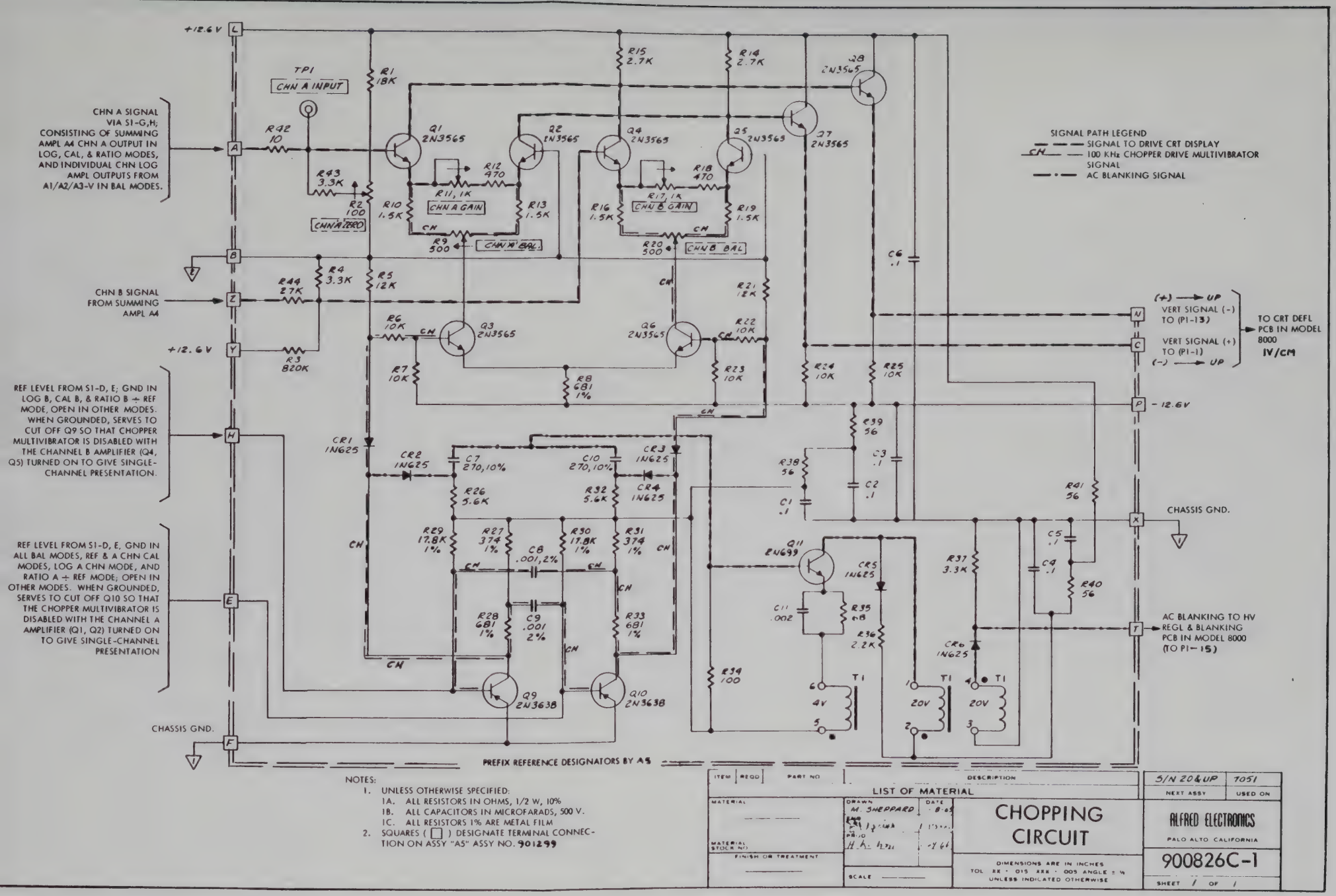
MATERIAL	DRAWN M. SHEPPARD	DATE 11-17-65	SUMMING AMPLIFIER
MATERIAL STOCK NO	ENG		
FINISH OR TREATMENT	PROD		DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE
	SCALE		

S/N 20-up	7051
NEXT ASSY	USED ON

ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900825C-1

SHEET 1 OF 1



NOTES:

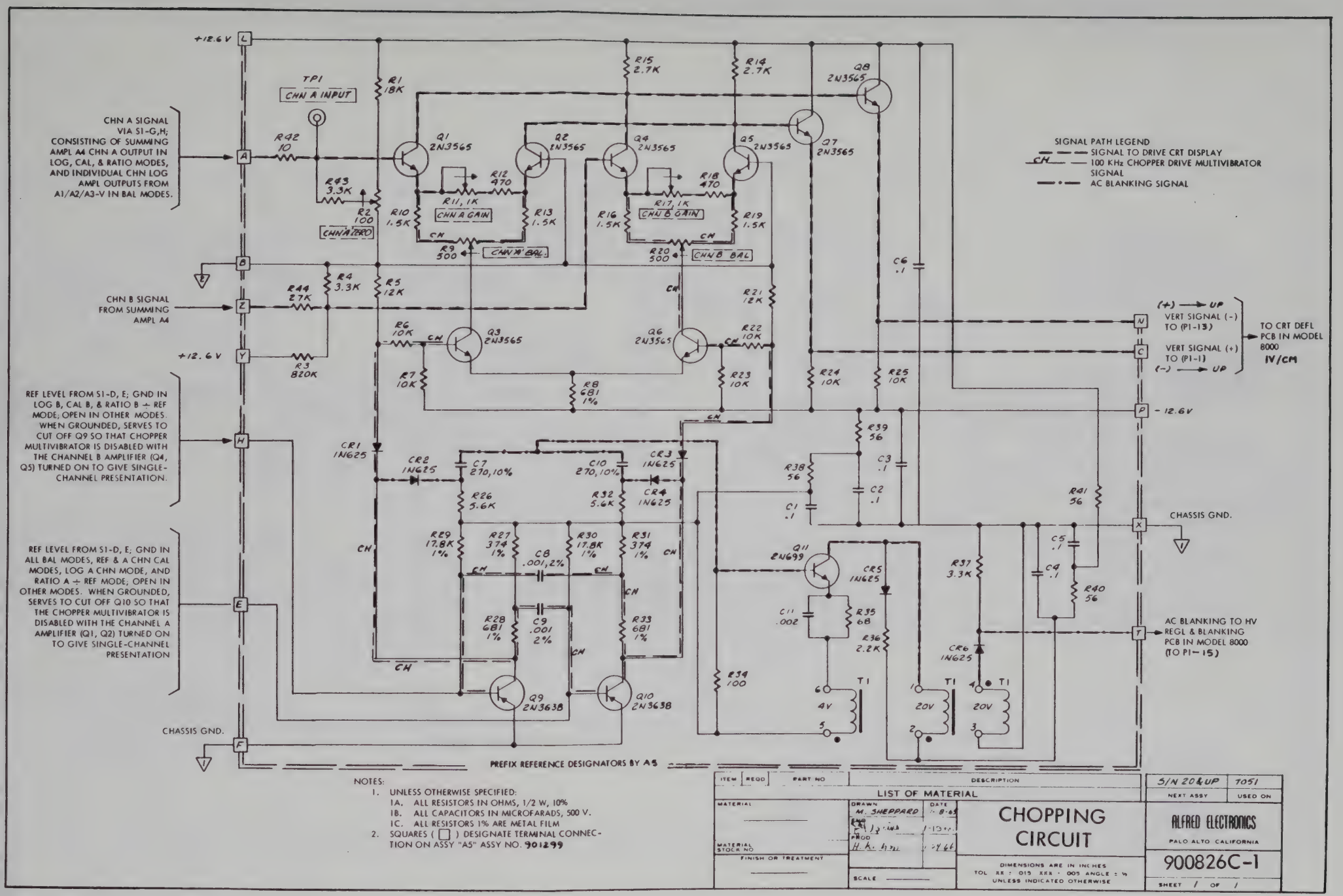
1. UNLESS OTHERWISE SPECIFIED:
   - 1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1B. ALL CAPACITORS IN MICROFARADS, 500 V.
   - 1C. ALL RESISTORS 1% ARE METAL FILM
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A5" ASSY NO. 901299

ITEM	REQD	PART NO	DESCRIPTION

LIST OF MATERIAL

MATERIAL	DRAWN M. SHEPPARD	DATE 8-65	CHOPPING CIRCUIT
MATERIAL STOCK NO	APVD H. A. Hall	2-66	ALFRED ELECTRONICS, PALO ALTO CALIFORNIA
FINISH OR TREATMENT	SCALE	DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE	900826C-1
			SHEET 1 OF 1

S/N 20&UP	7051
NEXT ASSY	USED ON

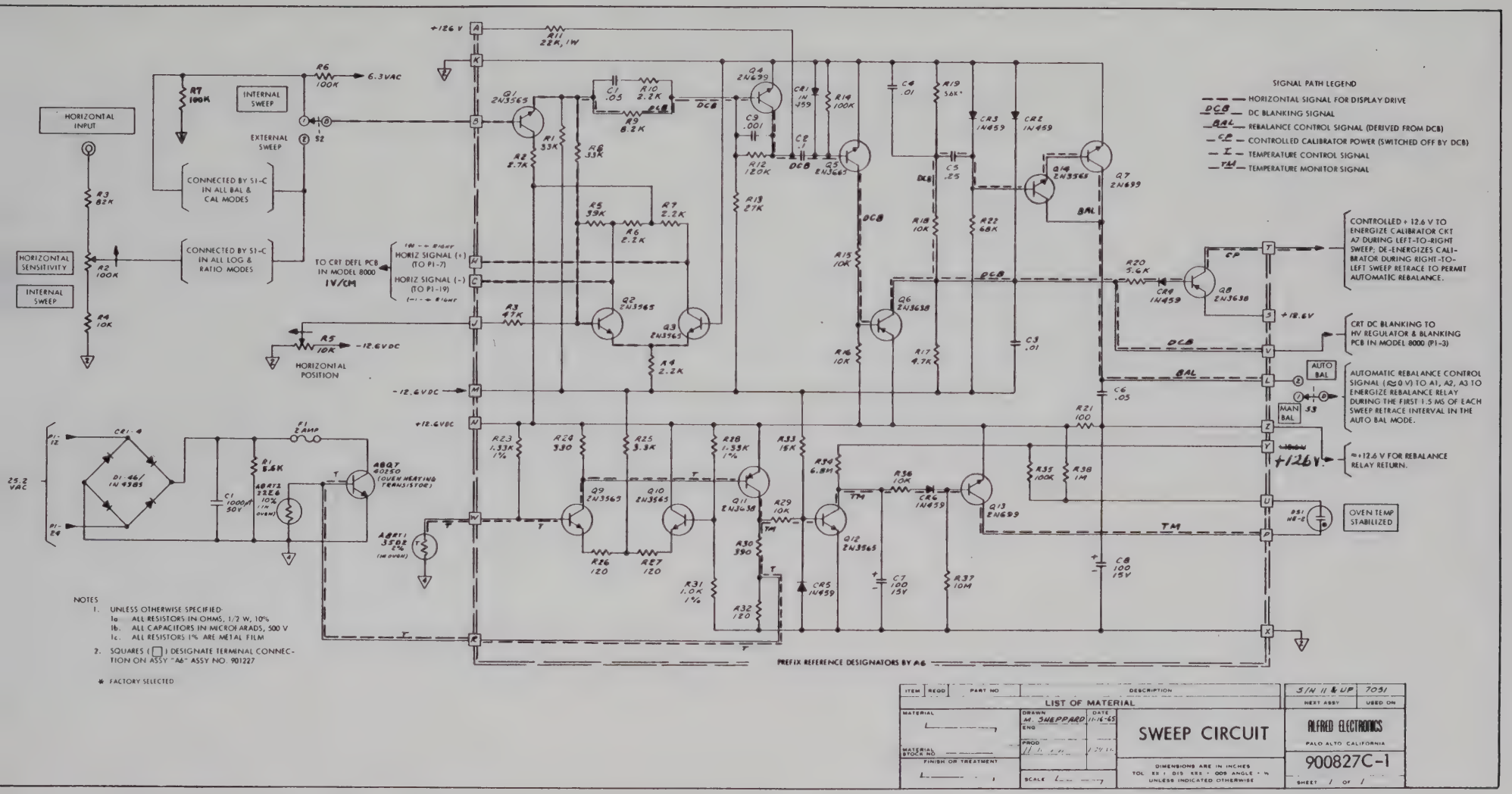


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - 1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1B. ALL CAPACITORS IN MICROFARADS, 500 V.
   - 1C. ALL RESISTORS 1% ARE METAL FILM
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A5" ASSY NO. 901299

ITEM	REQD	PART NO	DESCRIPTION
			LIST OF MATERIAL

S/N 204 UP	T051		
NEXT ASSY	USED ON		
MATERIAL	DRAWN M. SHEPPARD	DATE 7-8-65	CHOPPING CIRCUIT
MATERIAL STOCK NO	PROD H. A. [illegible]	DATE 7-9-65	ALFRED ELECTRONICS, PALO ALTO CALIFORNIA
FINISH OR TREATMENT	SCALE	DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE	900826C-1
			SHEET 1 OF 1


HORIZONTAL INPUT
HORIZONTAL SENSITIVITY
INTERNAL SWEEP
EXTERNAL SWEEP
INTERNAL SWEEP
CONNECTED BY S1-C IN ALL BAL & CAL MODES
CONNECTED BY S1-C IN ALL LOG & RATIO MODES
TO CRT DEFL PCB IN MODEL 8000
1V/CM
HORIZ SIGNAL (+) (TO P1-7)
HORIZ SIGNAL (-) (TO P1-19)
HORIZONTAL POSITION
+12.6 V
-12.6VDC
+12.6VDC
6.3VAC
25.2 VAC
SIGNAL PATH LEGEND
HORIZONTAL SIGNAL FOR DISPLAY DRIVE
DC BLANKING SIGNAL
REBALANCE CONTROL SIGNAL (DERIVED FROM DCB)
CONTROLLED CALIBRATOR POWER (SWITCHED OFF BY DCB)
TEMPERATURE CONTROL SIGNAL
TEMPERATURE MONITOR SIGNAL
CONTROLLED + 12.6 V TO ENERGIZE CALIBRATOR CKT A7 DURING LEFT-TO-RIGHT SWEEP; DE-ENERGIZES CALIBRATOR DURING RIGHT-TO-LEFT SWEEP RETRACE TO PERMIT AUTOMATIC REBALANCE.
+18.6V
CRT DC BLANKING TO HV REGULATOR & BLANKING PCB IN MODEL 8000 (P1-3)
AUTOMATIC REBALANCE CONTROL SIGNAL (≈0 V) TO A1, A2, A3 TO ENERGIZE REBALANCE RELAY DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL IN THE AUTO BAL MODE.
≈+12.6 V FOR REBALANCE RELAY RETURN.
OVEN TEMP STABILIZED
PREFIX REFERENCE DESIGNATORS BY A6

NOTES

1. UNLESS OTHERWISE SPECIFIED:
   - 1a. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1b. ALL CAPACITORS IN MICROFARADS, 500 V
   - 1c. ALL RESISTORS 1% ARE METAL FILM
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION ON ASSY "A6" ASSY NO. 901227

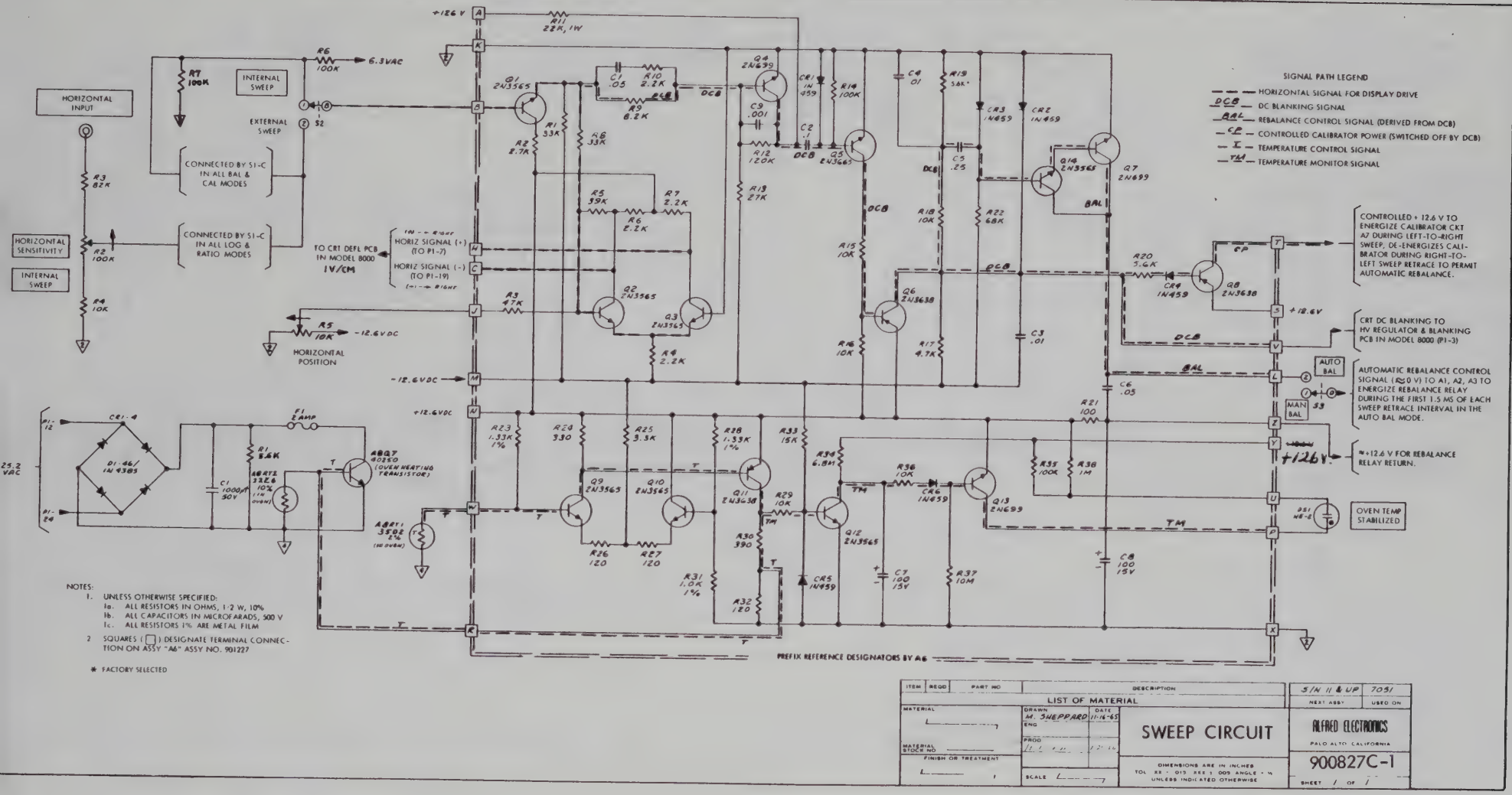
* FACTORY SELECTED

LIST OF MATERIAL

ITEM	REQD	PART NO	DESCRIPTION

MATERIAL	DRAWN M. SHEPPARD	DATE 11-16-65	SWEEP CIRCUIT
MATERIAL STOCK NO	ENG		
FINISH OR TREATMENT	PROD		DIMENSIONS ARE IN INCHES TOL XX ± .015 XXX ± .005 ANGLE ± ½ UNLESS INDICATED OTHERWISE
	SCALE		

S/N 11 & UP	7051
NEXT ASSY	USED ON
ALFRED ELECTRONICS, PALO ALTO CALIFORNIA	
900827C-1	
SHEET 1 OF 1	


SIGNAL PATH LEGEND
HORIZONTAL SIGNAL FOR DISPLAY DRIVE
DCB — DC BLANKING SIGNAL
BAL — REBALANCE CONTROL SIGNAL (DERIVED FROM DCB)
CP — CONTROLLED CALIBRATOR POWER (SWITCHED OFF BY DCB)
T — TEMPERATURE CONTROL SIGNAL
TM — TEMPERATURE MONITOR SIGNAL
HORIZONTAL INPUT
INTERNAL SWEEP
EXTERNAL SWEEP
CONNECTED BY S1-C IN ALL BAL & CAL MODES
CONNECTED BY S1-C IN ALL LOG & RATIO MODES
HORIZONTAL SENSITIVITY
INTERNAL SWEEP
HORIZONTAL POSITION
TO CRT DEFL PCB IN MODEL 8000
1V/CM
HORIZ SIGNAL (+) (TO P1-7)
HORIZ SIGNAL (-) (TO P1-19)
+12.6 V
6.3VAC
-12.6VDC
+12.6VDC
25.2 VAC
CONTROLLED + 12.6 V TO ENERGIZE CALIBRATOR CKT A7 DURING LEFT-TO-RIGHT SWEEP, DE-ENERGIZES CALIBRATOR DURING RIGHT-TO-LEFT SWEEP RETRACE TO PERMIT AUTOMATIC REBALANCE.
CRT DC BLANKING TO HV REGULATOR & BLANKING PCB IN MODEL 8000 (P1-3)
AUTOMATIC REBALANCE CONTROL SIGNAL (≈0 V) TO A1, A2, A3 TO ENERGIZE REBALANCE RELAY DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL IN THE AUTO BAL MODE.
≈+12.6 V FOR REBALANCE RELAY RETURN.
OVEN TEMP STABILIZED
AUTO BAL
MAN BAL
PREFIX REFERENCE DESIGNATORS BY A6

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   1a. ALL RESISTORS IN OHMS, 1/2 W, 10%
   1b. ALL CAPACITORS IN MICROFARADS, 500 V
   1c. ALL RESISTORS 1% ARE METAL FILM
2 SQUARES (□) DESIGNATE TERMINAL CONNECTION ON ASSY "A6" ASSY NO. 901227

* FACTORY SELECTED

ITEM	REQD	PART NO	DESCRIPTION

LIST OF MATERIAL

MATERIAL
MATERIAL STOCK NO
FINISH OR TREATMENT

DRAWN M. SHEPPARD 11-16-65
ENG
PROD
SCALE

SWEEP CIRCUIT

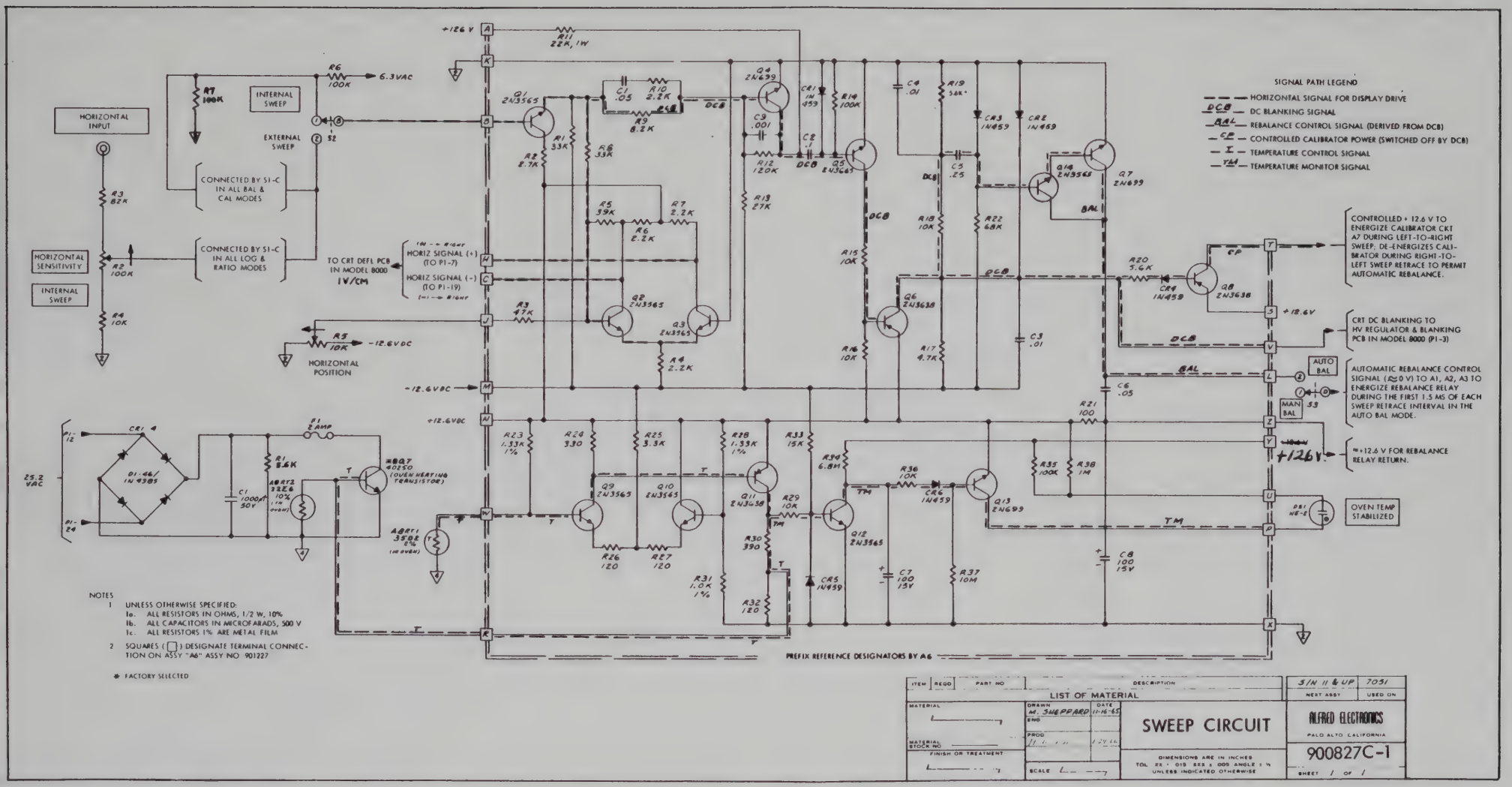
DIMENSIONS ARE IN INCHES
TOL XX ± .015 XXX ± .005 ANGLE ± ½
UNLESS INDICATED OTHERWISE

S/N 11 & UP | 7051
NEXT ASSY | USED ON

ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900827C-1

SHEET 1 OF 1


HORIZONTAL INPUT
HORIZONTAL SENSITIVITY
INTERNAL SWEEP
EXTERNAL SWEEP
CONNECTED BY S1-C IN ALL BAL & CAL MODES
CONNECTED BY S1-C IN ALL LOG & RATIO MODES
TO CRT DEFL PCB IN MODEL 8000
1V/CM
HORIZ SIGNAL (+) (TO P1-7)
HORIZ SIGNAL (-) (TO P1-19)
HORIZONTAL POSITION
-12.6VDC
+12.6VDC
6.3VAC
25.2 VAC
SIGNAL PATH LEGEND
HORIZONTAL SIGNAL FOR DISPLAY DRIVE
DC BLANKING SIGNAL
REBALANCE CONTROL SIGNAL (DERIVED FROM DCB)
CONTROLLED CALIBRATOR POWER (SWITCHED OFF BY DCB)
TEMPERATURE CONTROL SIGNAL
TEMPERATURE MONITOR SIGNAL
CONTROLLED + 12.6 V TO ENERGIZE CALIBRATOR CKT A7 DURING LEFT-TO-RIGHT SWEEP; DE-ENERGIZES CALIBRATOR DURING RIGHT-TO-LEFT SWEEP RETRACE TO PERMIT AUTOMATIC REBALANCE.
CRT DC BLANKING TO HV REGULATOR & BLANKING PCB IN MODEL 8000 (P1-3)
AUTOMATIC REBALANCE CONTROL SIGNAL (≅0 V) TO A1, A2, A3 TO ENERGIZE REBALANCE RELAY DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL IN THE AUTO BAL MODE.
*+12.6 V FOR REBALANCE RELAY RETURN.
+12.6V*
OVEN TEMP STABILIZED
AUTO BAL
MAN BAL
PREFIX REFERENCE DESIGNATORS BY A6

NOTES

1 UNLESS OTHERWISE SPECIFIED:
- 1a. ALL RESISTORS IN OHMS, 1/2 W, 10%
- 1b. ALL CAPACITORS IN MICROFARADS, 500 V
- 1c. ALL RESISTORS 1% ARE METAL FILM

2 SQUARES (□) DESIGNATE TERMINAL CONNECTION ON ASSY "A6" ASSY NO 901227

* FACTORY SELECTED

ITEM	REQD	PART NO	DESCRIPTION

LIST OF MATERIAL

MATERIAL	DRAWN M. SHEPPARD	DATE 11-16-65
MATERIAL STOCK NO	ENG	
FINISH OR TREATMENT	PROD	
	SCALE	

SWEEP CIRCUIT

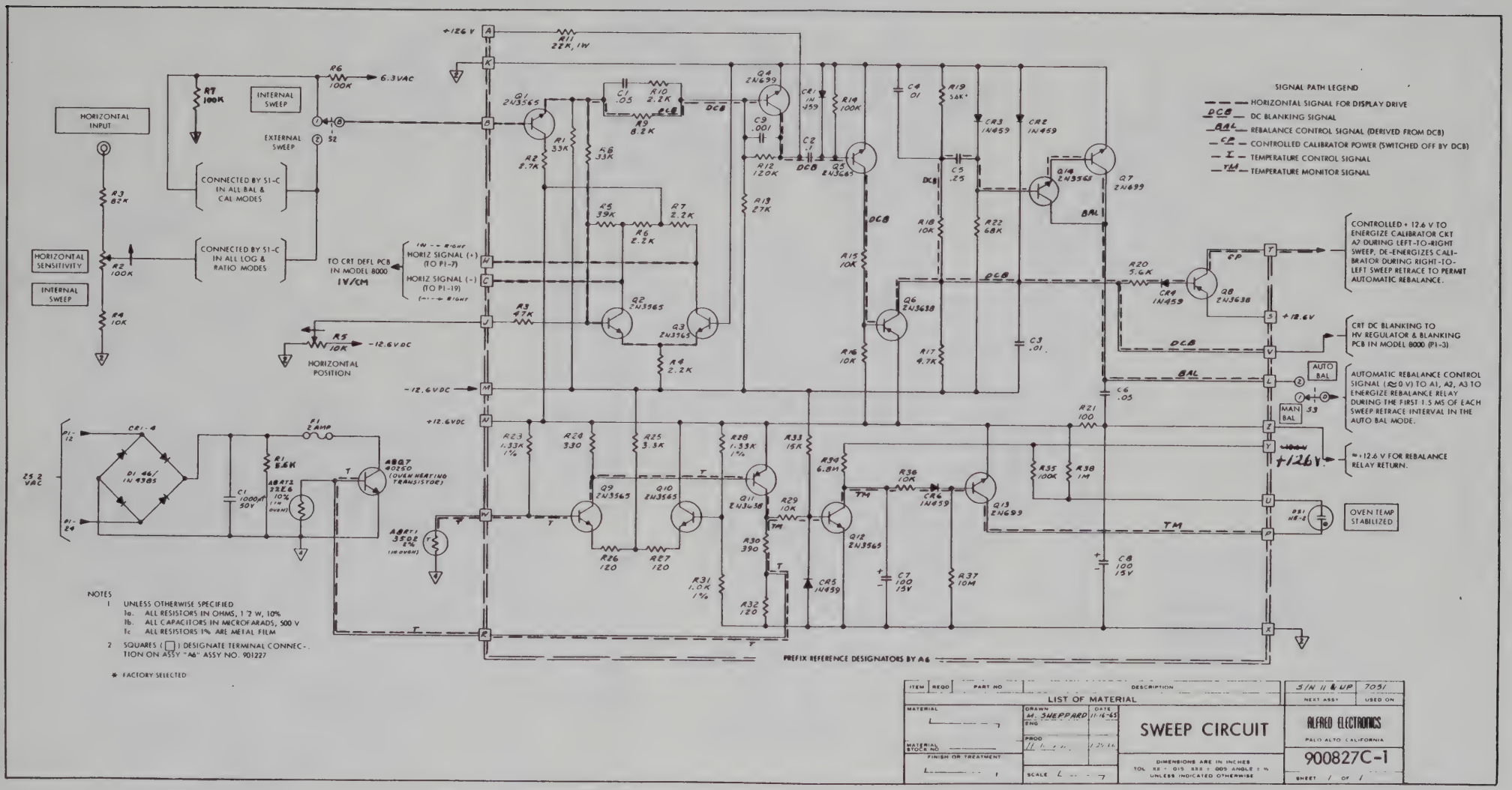
DIMENSIONS ARE IN INCHES
TOL .XX ± .010 .XXX ± .005 ANGLE ± ½°
UNLESS INDICATED OTHERWISE

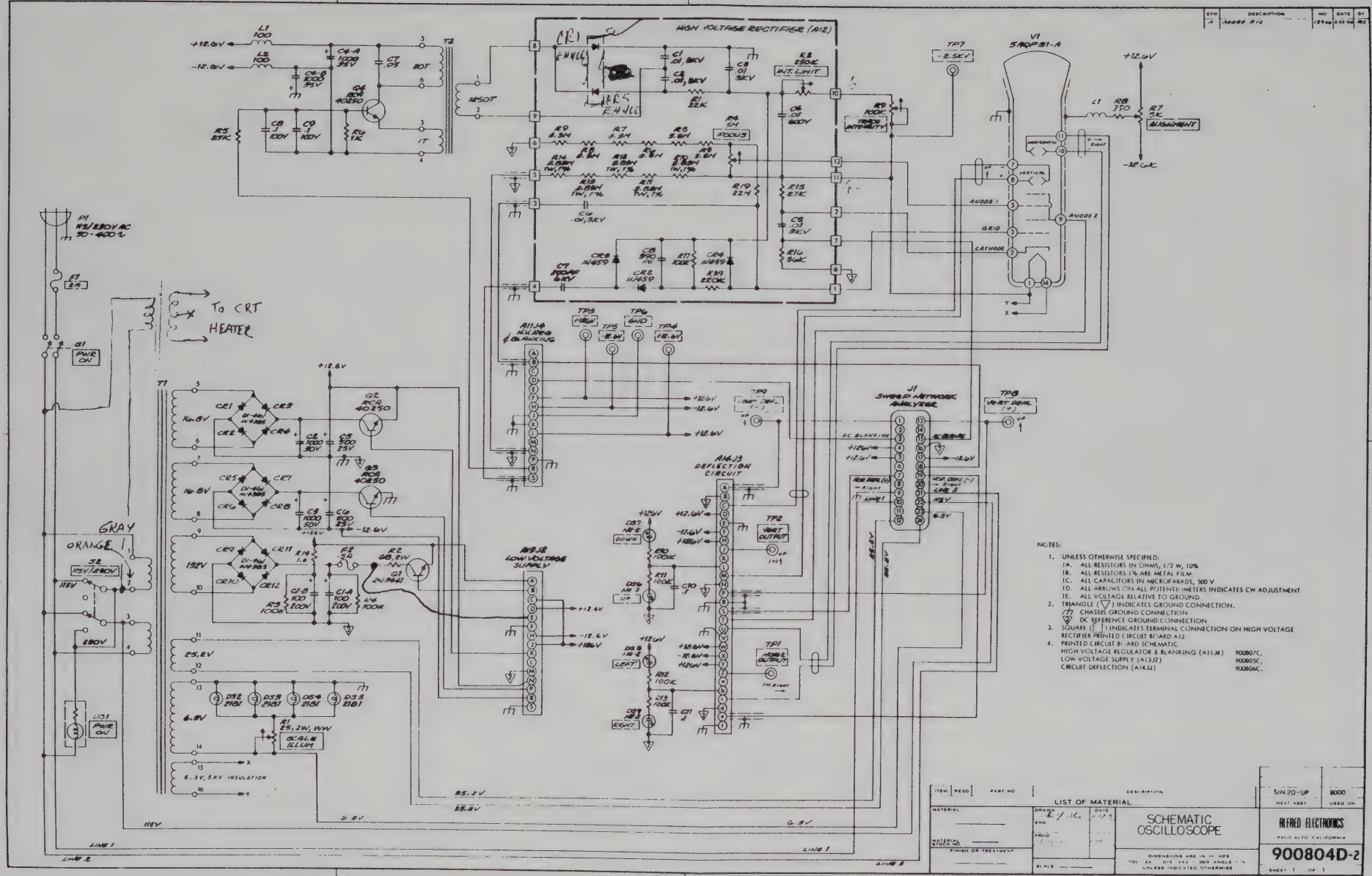
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

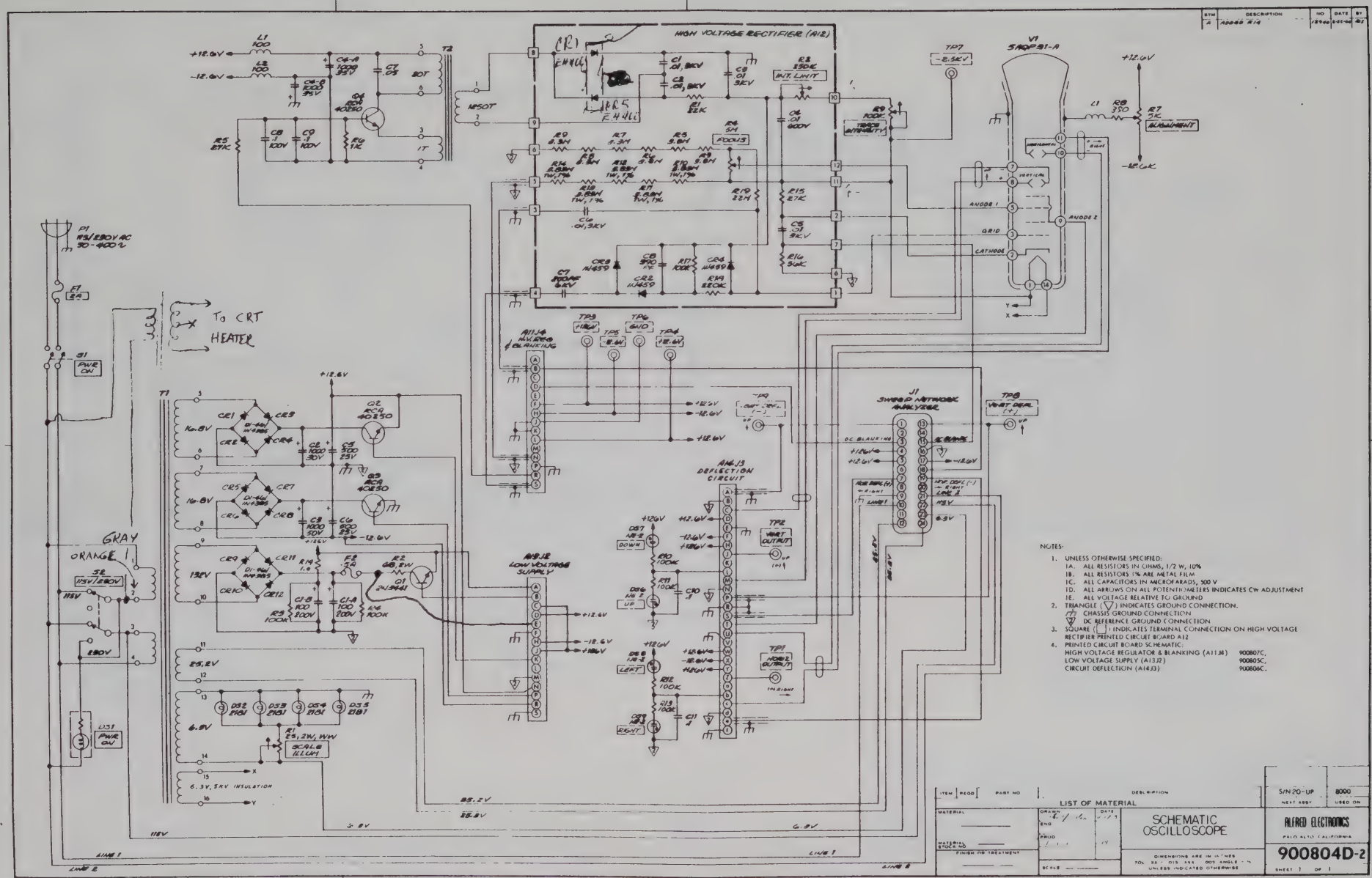
900827C-1

SHEET 1 OF 1

S/N 11 & UP	7051
NEXT ASSY	USED ON


SIGNAL PATH LEGEND
HORIZONTAL SIGNAL FOR DISPLAY DRIVE
DCB — DC BLANKING SIGNAL
BAL — REBALANCE CONTROL SIGNAL (DERIVED FROM DCB)
CP — CONTROLLED CALIBRATOR POWER (SWITCHED OFF BY DCB)
I — TEMPERATURE CONTROL SIGNAL
TM — TEMPERATURE MONITOR SIGNAL
HORIZONTAL INPUT
INTERNAL SWEEP
EXTERNAL SWEEP
HORIZONTAL SENSITIVITY
HORIZONTAL POSITION
CONNECTED BY S1-C IN ALL BAL & CAL MODES
CONNECTED BY S1-C IN ALL LOG & RATIO MODES
TO CRT DEFL PCB IN MODEL 8000
1V/CM
HORIZ SIGNAL (+) (TO P1-7)
HORIZ SIGNAL (-) (TO P1-19)
+12.6 V
-12.6VDC
+12.6VDC
6.3VAC
25.2 VAC
CONTROLLED + 12.6 V TO ENERGIZE CALIBRATOR CKT A2 DURING LEFT-TO-RIGHT SWEEP, DE-ENERGIZES CALIBRATOR DURING RIGHT-TO-LEFT SWEEP RETRACE TO PERMIT AUTOMATIC REBALANCE.
CRT DC BLANKING TO HV REGULATOR & BLANKING PCB IN MODEL 8000 (P1-3)
AUTOMATIC REBALANCE CONTROL SIGNAL (≥0 V) TO A1, A2, A3 TO ENERGIZE REBALANCE RELAY DURING THE FIRST 1.5 MS OF EACH SWEEP RETRACE INTERVAL IN THE AUTO BAL MODE.
AUTO BAL
MAN BAL
+12.6 V FOR REBALANCE RELAY RETURN.
OVEN TEMP STABILIZED
PREFIX REFERENCE DESIGNATORS BY A6
NOTES
1 UNLESS OTHERWISE SPECIFIED
1a. ALL RESISTORS IN OHMS, 1/2 W, 10%
1b. ALL CAPACITORS IN MICROFARADS, 500 V
1c ALL RESISTORS 1% ARE METAL FILM
2 SQUARES (□) DESIGNATE TERMINAL CONNECTION ON ASSY "A6" ASSY NO. 901227
* FACTORY SELECTED
LIST OF MATERIAL
SWEEP CIRCUIT
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA
900827C-1
DRAWN M. SHEPPARD
DATE 11-16-65
DIMENSIONS ARE IN INCHES
SHEET 1 OF 1


HIGH VOLTAGE RECTIFIER (A12)
A11J4 BLANKING
A11J3 LOW VOLTAGE SUPPLY
A14J3 DEFLECTION CIRCUIT
J1 SWITCHED NETWORK ANALYZER
V1 5AQP31-A
To CRT HEATER
GRAY
ORANGE
INTENSITY
FOCUS
ASTIGMATISM
HORIZONTAL
VERTICAL
ANODE 1
ANODE 2
GRID
CATHODE
ALIGNMENT
DC BLANKING
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
1B. ALL RESISTORS 1% ARE METAL FILM
1C. ALL CAPACITORS IN MICROFARADS, 500 V
1D. ALL ARROWS ON ALL POTENTIOMETERS INDICATES CW ADJUSTMENT
1E. ALL VOLTAGE RELATIVE TO GROUND
2. TRIANGLE (▽) INDICATES GROUND CONNECTION.
⏚ CHASSIS GROUND CONNECTION
▽ DC REFERENCE GROUND CONNECTION
3. SQUARE ( ) INDICATES TERMINAL CONNECTION ON HIGH VOLTAGE RECTIFIER PRINTED CIRCUIT BOARD A12
4. PRINTED CIRCUIT BOARD SCHEMATIC
HIGH VOLTAGE REGULATOR & BLANKING (A11J4) 900807C,
LOW VOLTAGE SUPPLY (A13J2) 900805C,
CIRCUIT DEFLECTION (A14J3) 900806C.
LIST OF MATERIAL
SCHEMATIC OSCILLOSCOPE
ALFRED ELECTRONICS
900804D-2
S/N 20-UP
8000


HIGH VOLTAGE RECTIFIER (A12)
T1
T2
L1
L2
CR1
Q1
Q2
Q3
Q4
T1 3
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
Q2 RCA 40250
Q3 RCA 40250
Q4 RCA 40250
Q1 2N3441
C1
C2
C3
C4-A
C4-B
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
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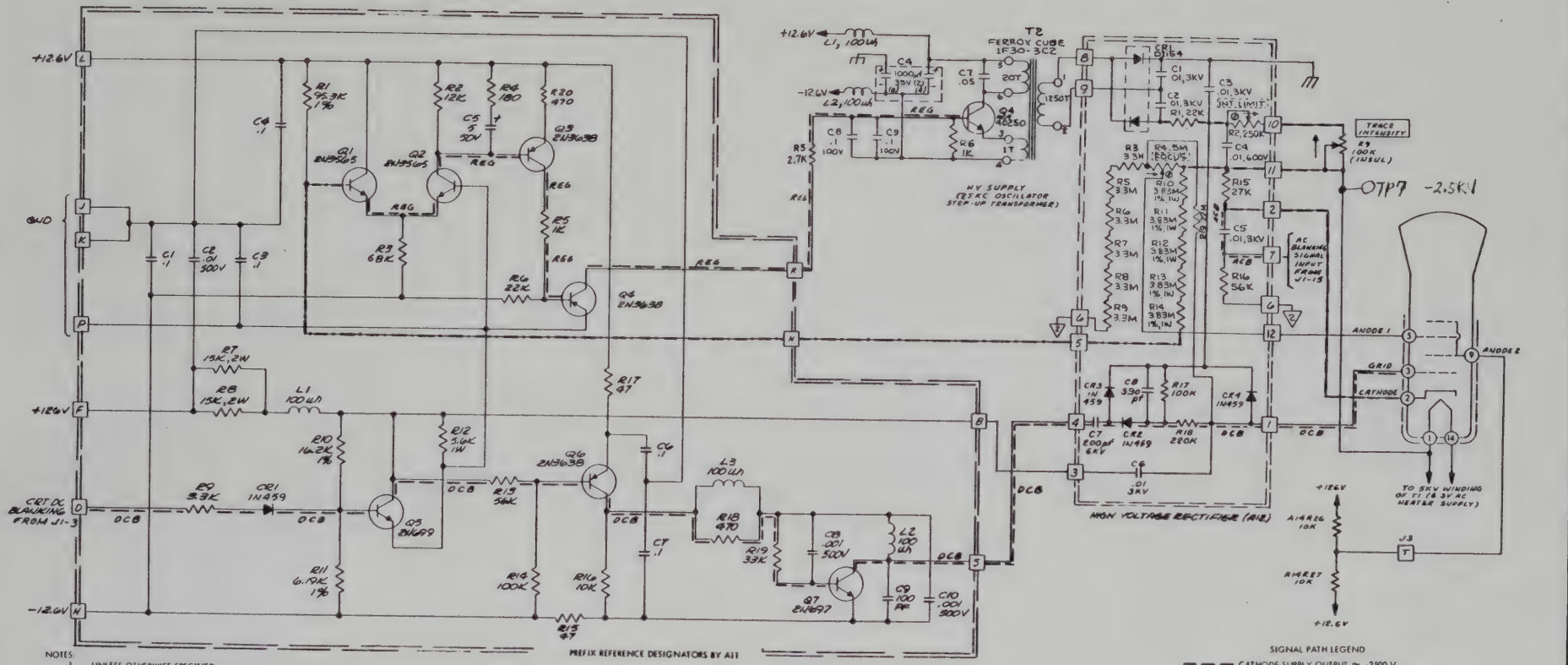
R36
R37
R38
R39
R40



NOTES:
1. UNLESS OTHERWISE SPECIFIED-
   1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   1B. ALL CAPACITORS IN MICROFARADS, 100 V
   1C. ALL RESISTORS 1% ARE METAL FILM
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION

SIGNAL PATH LEGEND
- CATHODE SUPPLY OUTPUT ≈ -2500 V
- FEEDBACK FROM CATHODE SUPPLY OUTPUT TO HV REGULATOR
- REG — HV REGULATOR SIGNAL TO CONTROL HV SUPPLY OSCILLATION AMPLITUDE
- ACB — AC BLANKING SIGNAL FROM A5 IN PLUG-IN UNIT
- DCB — DC BLANKING SIGNAL FROM A6 IN PLUG-IN UNIT

ITEM	REQD	PART NO	DESCRIPTION	SN 11-UP	8000
			LIST OF MATERIAL	NEXT ASSY	USED ON

MATERIAL
MATERIAL SPEC NO.
FINISH OR TREATMENT

DRAWN — DATE 8-10-65
ENG — DATE 1-13-66
PROD — DATE 1-24-66
SCALE

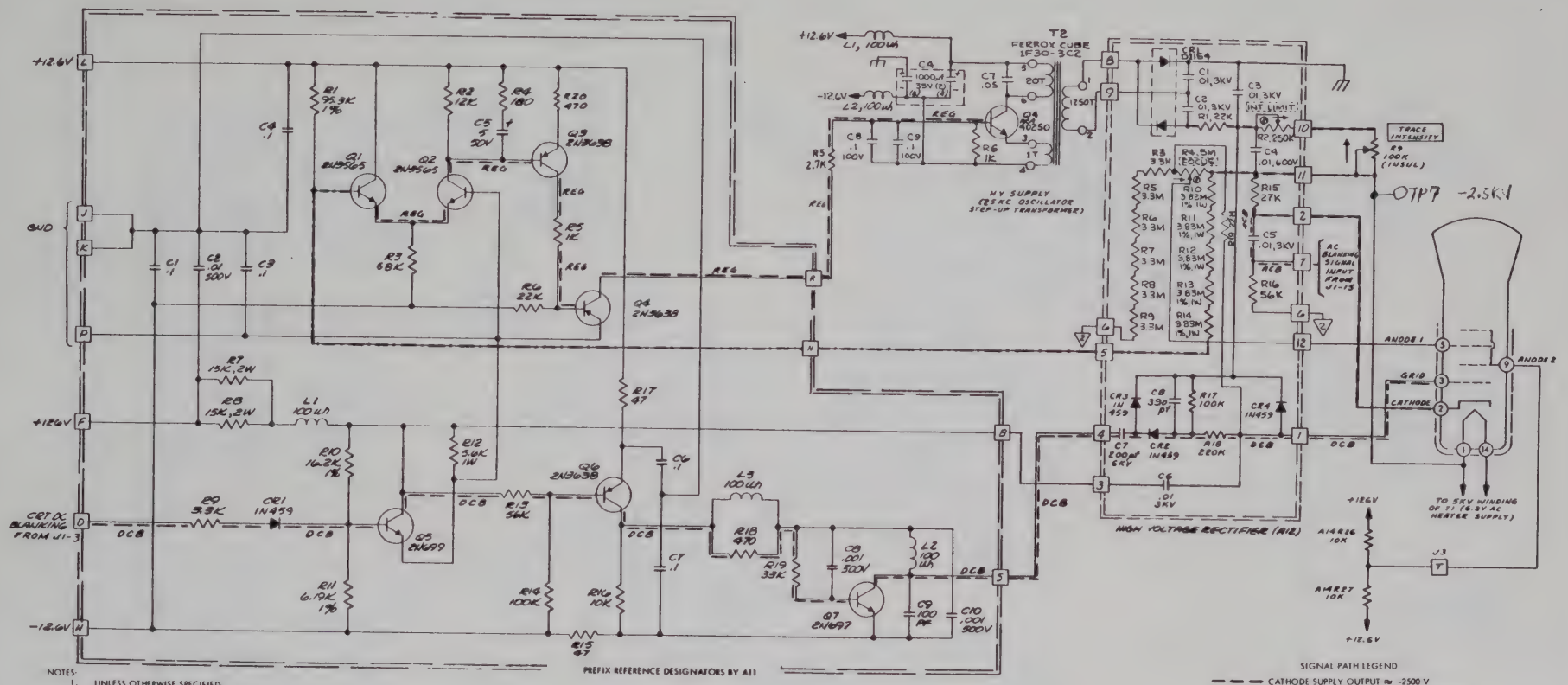
HIGH VOLTAGE REG. & BLANKING

DIMENSIONS ARE IN INCHES
TOL .XX ± .015 .XXX ± .005 ANGLE ± 1°
UNLESS INDICATED OTHERWISE

ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900807C-1

SHEET 1 OF 1


+12.6V
GND
-12.6V
CRT DC BLANKING FROM J1-3
T2 FERROX CUBE 1F30-3C2
HV SUPPLY (83KC OSCILLATOR STEP-UP TRANSFORMER)
HIGH VOLTAGE RECTIFIER (A12)
TRACE INTENSITY
AC BLANKING SIGNAL INPUT FROM J1-15
OTP7 -2.5KV
ANODE 1
ANODE 2
GRID
CATHODE
TO 5KV WINDING OF T1 (6.3V AC HEATER SUPPLY)
SIGNAL PATH LEGEND
CATHODE SUPPLY OUTPUT ≈ -2500 V
FEEDBACK FROM CATHODE SUPPLY OUTPUT TO HV REGULATOR
REG HV REGULATOR SIGNAL TO CONTROL HV SUPPLY OSCILLATION AMPLITUDE
ACB AC BLANKING SIGNAL FROM A5 IN PLUG-IN UNIT
DCB DC BLANKING SIGNAL FROM A6 IN PLUG-IN UNIT

NOTES

1. UNLESS OTHERWISE SPECIFIED
   - 1A. ALL RESISTORS IN OHMS, 1/2 W, 10%
   - 1B. ALL CAPACITORS IN MICROFARADS, 100 V
   - 1C. ALL RESISTORS 1% ARE METAL FILM
2. SQUARES (☐) DESIGNATE TERMINAL CONNECTION

PREFIX REFERENCE DESIGNATORS BY A11

ASSY A11 ASSEMBLY No. 950917

LIST OF MATERIAL

ITEM	REQD	PART NO	DESCRIPTION

SAV 11-UP | 8000 | NEXT ASSY | USED ON

MATERIAL | MATERIAL STOCK NO | FINISH OR TREATMENT

DRAWN | DATE 12-10-65
ENGR | DATE 1-13-66
PROD | DATE 1-27-66
SCALE

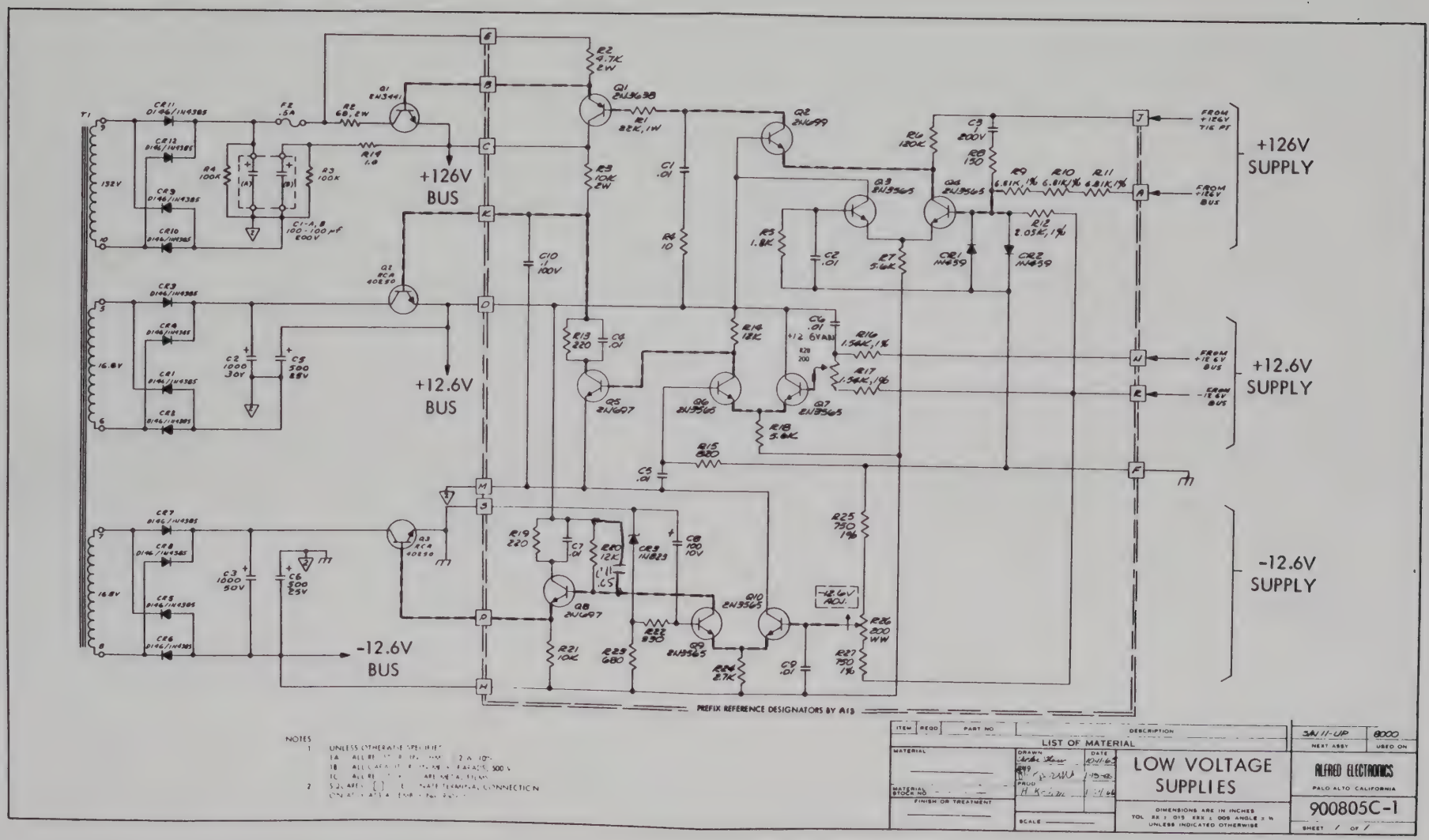
HIGH VOLTAGE REG. & BLANKING

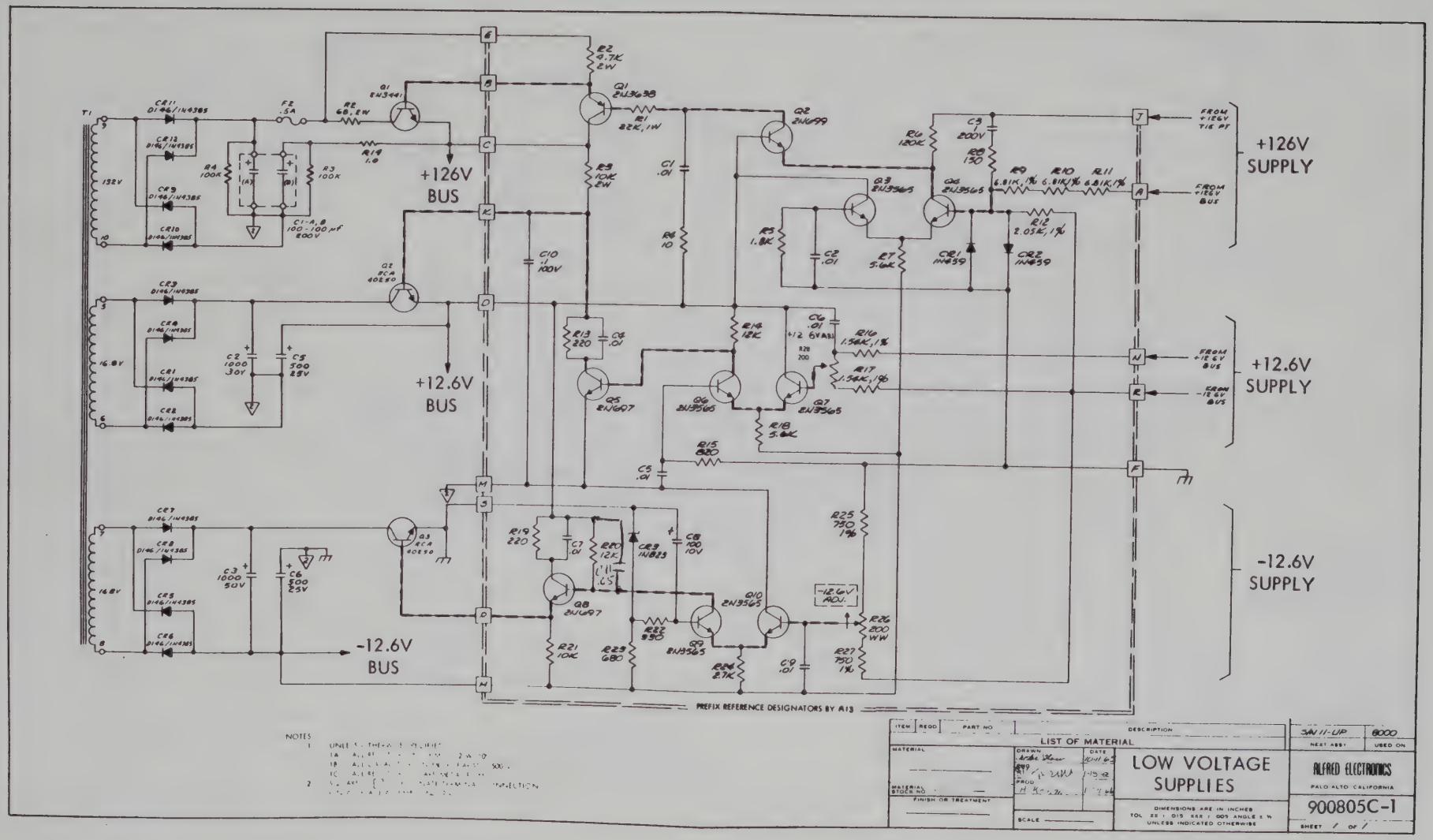
DIMENSIONS ARE IN INCHES
TOL .XX ± .015 .XXX ± .005 ANGLE ± ½
UNLESS INDICATED OTHERWISE

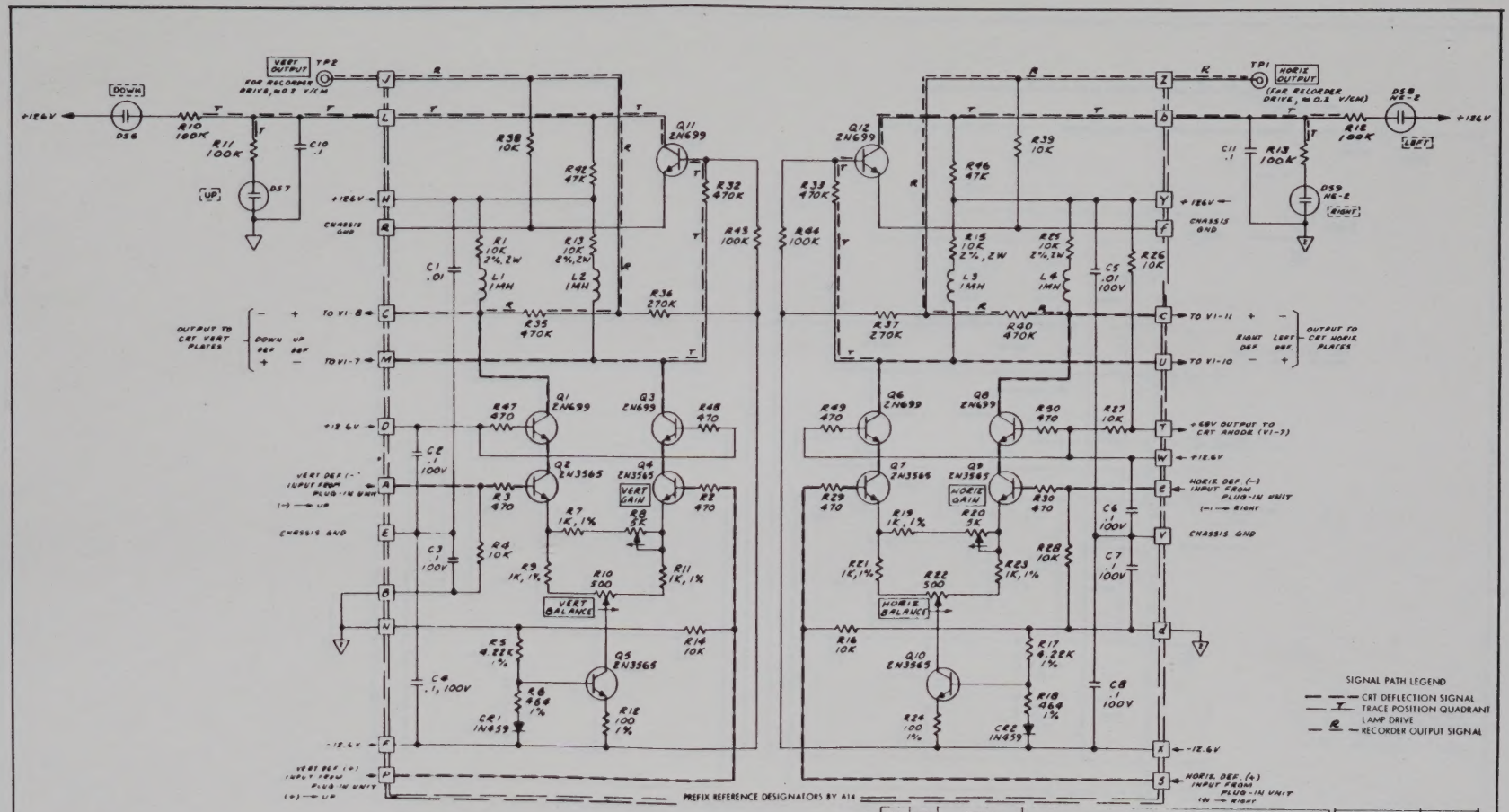
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA

900807C-1

SHEET 1 OF 1


+126V BUS
+12.6V BUS
-12.6V BUS
+126V SUPPLY
+12.6V SUPPLY
-12.6V SUPPLY
PREFIX REFERENCE DESIGNATORS BY A1B
LOW VOLTAGE SUPPLIES
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA
900805C-1
LIST OF MATERIAL
NOTES


+126V BUS
+12.6V BUS
-12.6V BUS
+126V SUPPLY
+12.6V SUPPLY
-12.6V SUPPLY
PREFIX REFERENCE DESIGNATORS BY A13
LOW VOLTAGE SUPPLIES
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA
900805C-1
LIST OF MATERIAL



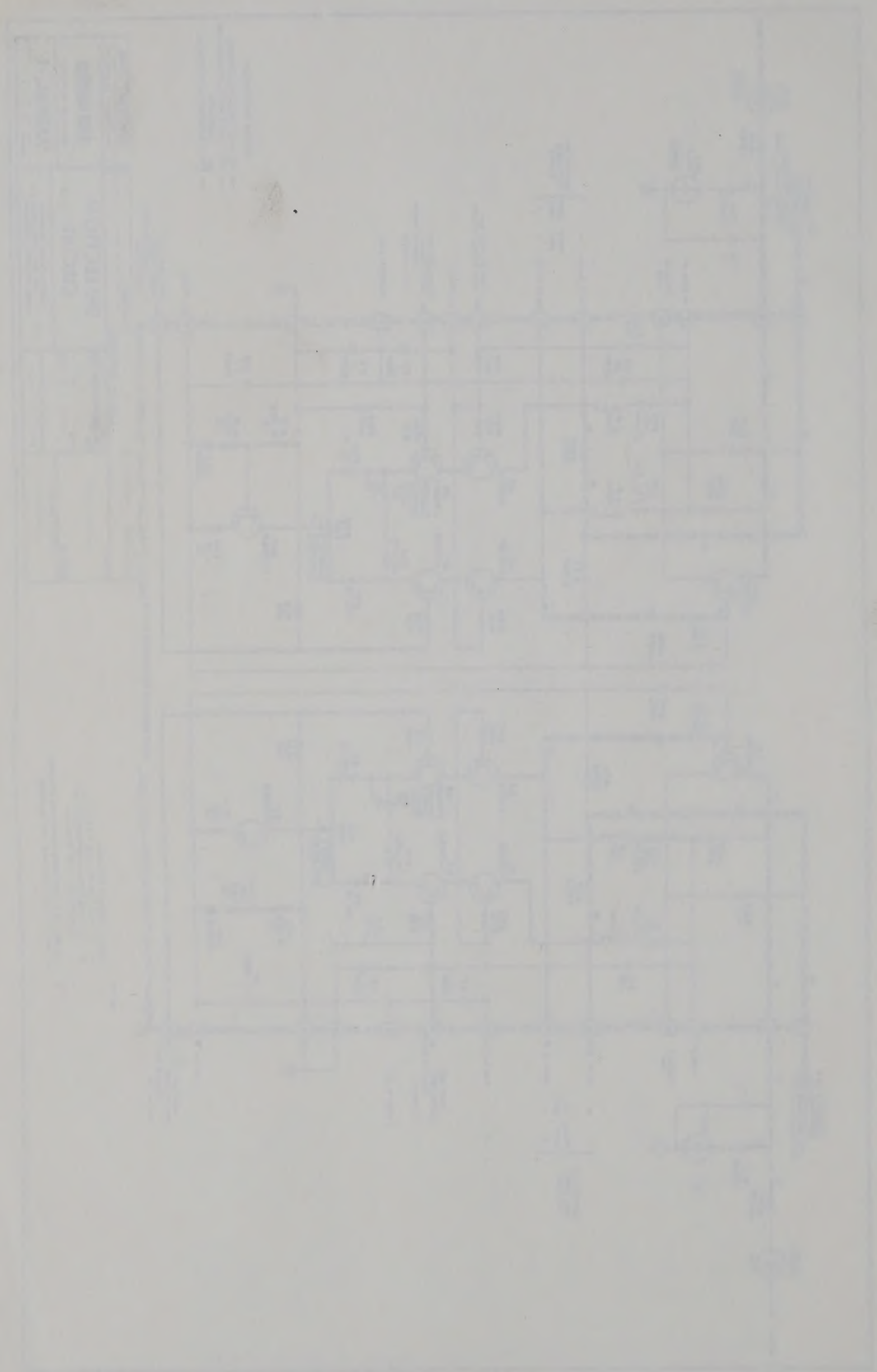
NOTES

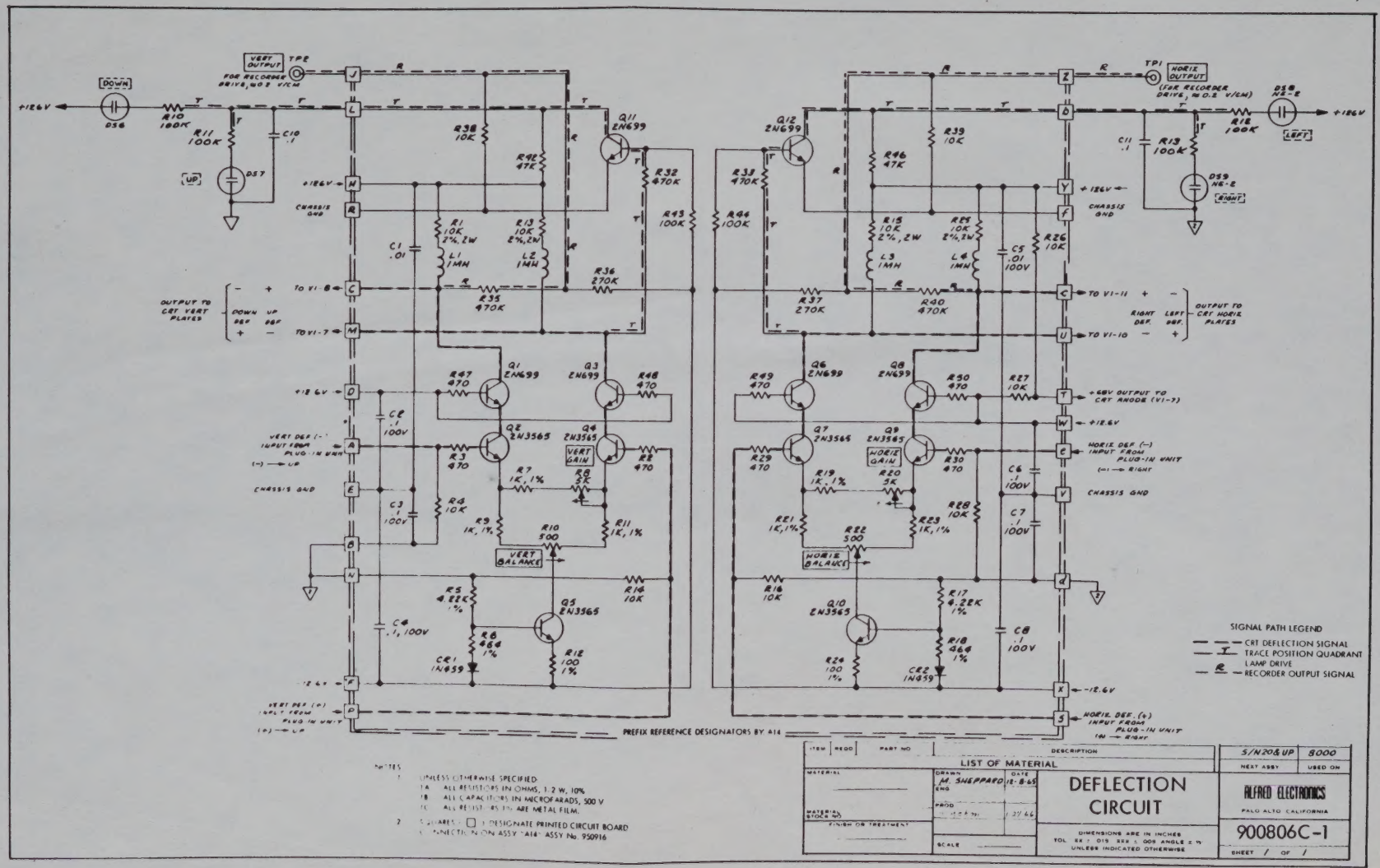
1. UNLESS OTHERWISE SPECIFIED:
   1A ALL RESISTORS IN OHMS, 1/2 W, 10%
   1B ALL CAPACITORS IN MICROFARADS, 500 V
   1C ALL RESISTORS 1% ARE METAL FILM.
2. SQUARES (☐) DESIGNATE PRINTED CIRCUIT BOARD CONNECTION ON ASSY "A14" ASSY No. 950916

ITEM	REQD	PART NO	DESCRIPTION
	1		LIST OF MATERIAL

MATERIAL	DRAWN M. SHEPPARD	DATE 12-8-65	DEFLECTION CIRCUIT
WAFER EL STOCK NO.	ENG		
FINISH OR TREATMENT	PROD		
	SCALE		DIMENSIONS ARE IN INCHES TOL .XX ± .015 .XXX ± .005 ANGLE ± ½° UNLESS INDICATED OTHERWISE

S/N 205 UP	8000
NEXT ASSY	USED ON
ALFRED ELECTRONICS	PALO ALTO CALIFORNIA
900806C-1	
SHEET 1 OF 1	




VERT OUTPUT
FOR RECORDER DRIVE, ≈0.2 V/CM
TP2
HORIZ OUTPUT
(FOR RECORDER DRIVE, ≈0.2 V/CM)
TP1
DOWN
UP
LEFT
RIGHT
+12.6V
-12.6V
CHASSIS GND
OUTPUT TO CRT VERT PLATES
OUTPUT TO CRT HORIZ PLATES
+68V OUTPUT TO CRT ANODE (V1-7)
VERT DEF (-) INPUT FROM PLUG-IN UNIT
HORIZ DEF (-) INPUT FROM PLUG-IN UNIT
VERT DEF (+) INPUT FROM PLUG-IN UNIT
HORIZ DEF (+) INPUT FROM PLUG-IN UNIT
VERT GAIN
HORIZ GAIN
VERT BALANCE
HORIZ BALANCE
SIGNAL PATH LEGEND
CRT DEFLECTION SIGNAL
TRACE POSITION QUADRANT
LAMP DRIVE
RECORDER OUTPUT SIGNAL
PREFIX REFERENCE DESIGNATORS BY A14
NOTES
1. UNLESS OTHERWISE SPECIFIED:
1A. ALL RESISTORS IN OHMS, 1-2 W, 10%
1B. ALL CAPACITORS IN MICROFARADS, 500 V
1C. ALL RESISTORS 1% ARE METAL FILM.
2. SHADED ☐ DESIGNATE PRINTED CIRCUIT BOARD CONNECTION ASSY "A14" ASSY No. 950916
LIST OF MATERIAL
DEFLECTION CIRCUIT
M. SHEPPARD
12-8-65
ALFRED ELECTRONICS
PALO ALTO CALIFORNIA
900806C-1
S/N 20& UP
8000
SHEET 1 OF 1